FSC-BT502

v2.1+EDR Bluetooth Module Data Sheet

Document Type:	FSC-BT502
Document Version:	V1.0
Release Date:	May 20 . 2016

Shenzhen Feasycom Technology Co.,Ltd.

Telephone: 86-755-27924639

www.feasycom.com

Release Record

Version Number	Release Date	Comments
Revision 1.0	2016-05-20	First Release

1. INTRODUCTION

FSC-BT502 is a small form factor, low power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to integrate into fully certified embedded Bluetooth solutions.

With AT+™ programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate for distances to 10M.

The module is an appropriate product for designers who want to add wireless capability to their products.

1.1 Block Diagram

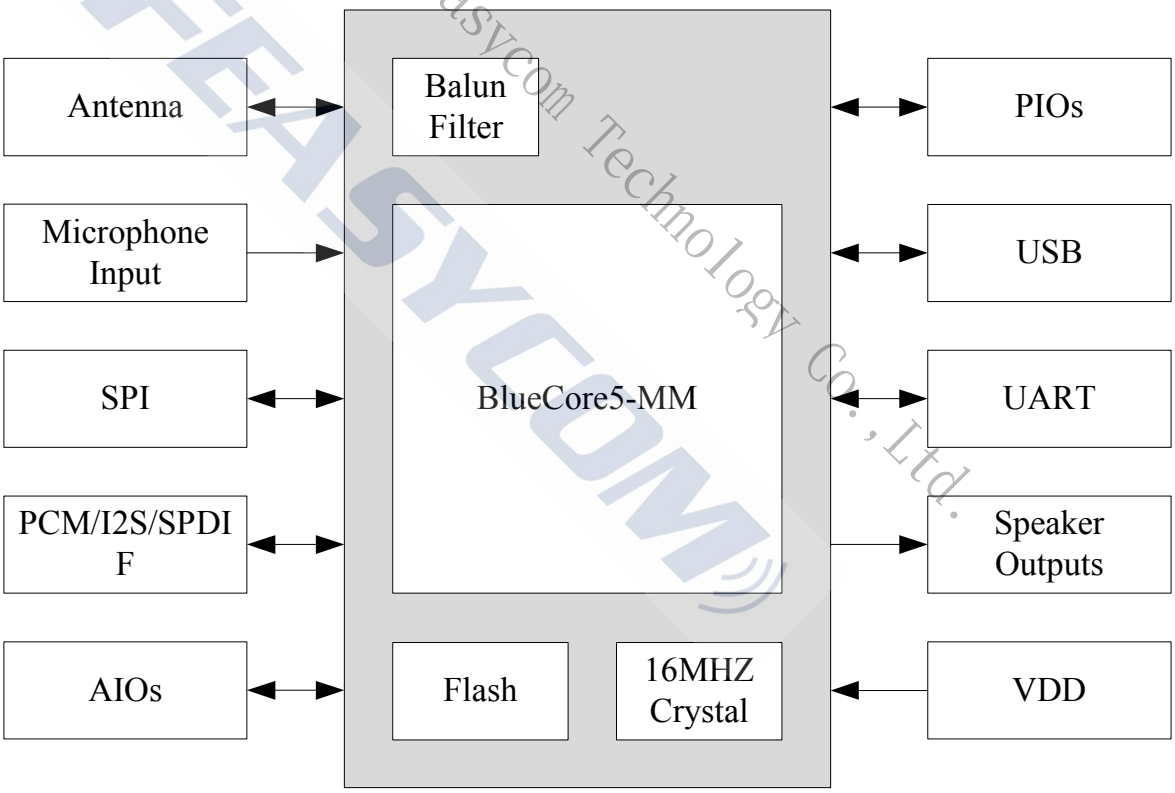

Figure 1: Block Diagram

1.2 Features

- Bluetooth v2.1+EDR, Class 2
- Profiles including HS/HF, A2DP, AVRCP, OPP, DUN, SPP, etc.
- UART and USB programming and data interfaces
- Small form factor
- SMT pads for easy and reliable PCB mounting
- RoHS compliant
- APTX (optional)

1.3 Application

- High quality stereo headsets
- High quality mono headsets
- Hands-free car kits
- Wireless speakers
- Bluetooth-Enable Automotive Dashboards
- VOIP handsets
- Analogue and USB Multimedia Dongles
- Medical devices
- Barcode and RFID scanners

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chipset	BC05 MM
Module	FSC-BT502
Dimension	21mm(L) x 13.5mm(W) x 2.0mm(H)
BT Standard	Bluetooth2.1+EDR, Class II
RF TX Output Power	4dBm
Sensitivity	-86dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	16MHz
Hopping	1600hops/sec, 1MHz channel space
RF Input Impedance	50 ohms
Major Interface	• UART, PIO, AIO, USB, SPI, Speaker, Microphone, etc. • Antenna
Profile	HS/HF, A2DP, AVRCP, OPP, DUN, SPP, etc. detailed profiles depends on the firmware
Voice Processor	64MIPS Kalimba with cVc support
Power	
Supply Voltage	3V3_INPUT=3.0~3.6V Volt DC
Working Current	Depends on profiles, 30mA typical
Standby Current	<1mA
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

3.1 Physical Dimensions

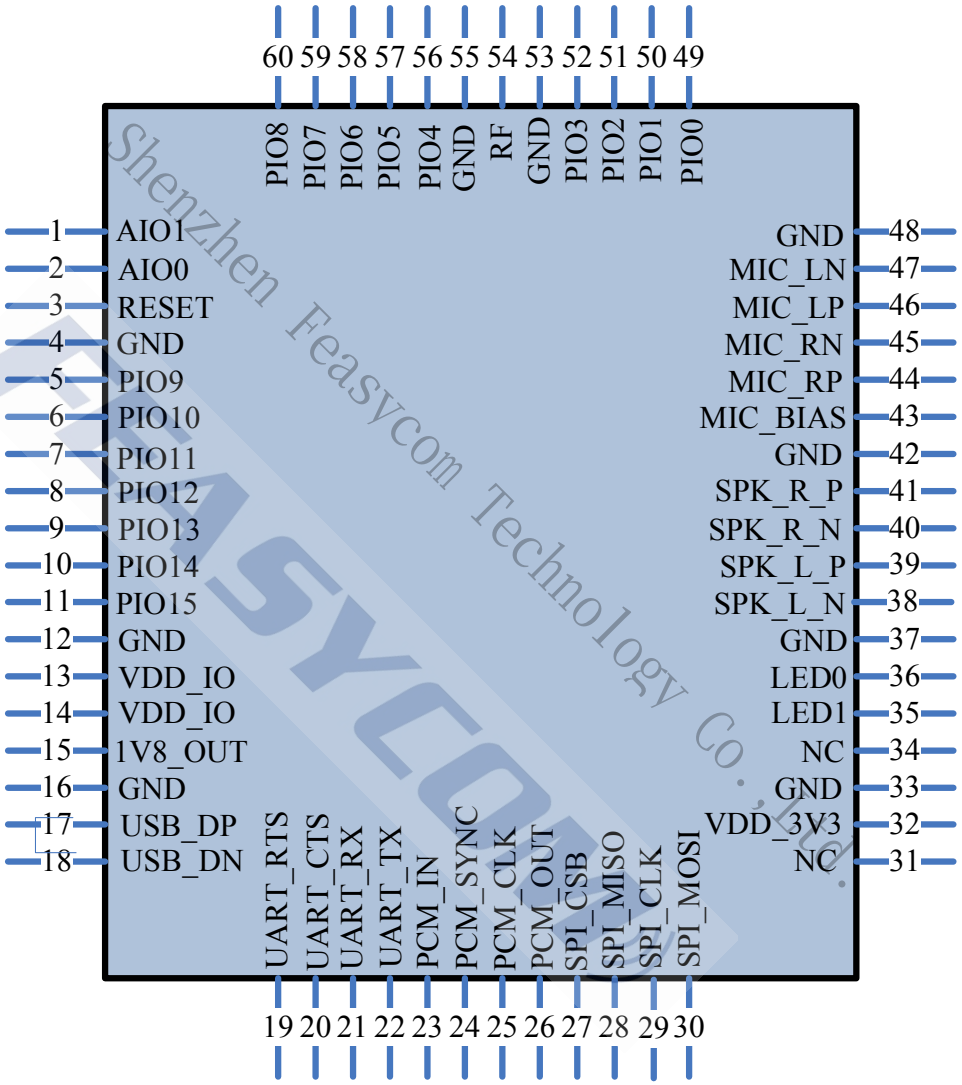

Figure 2: PIN Diagram

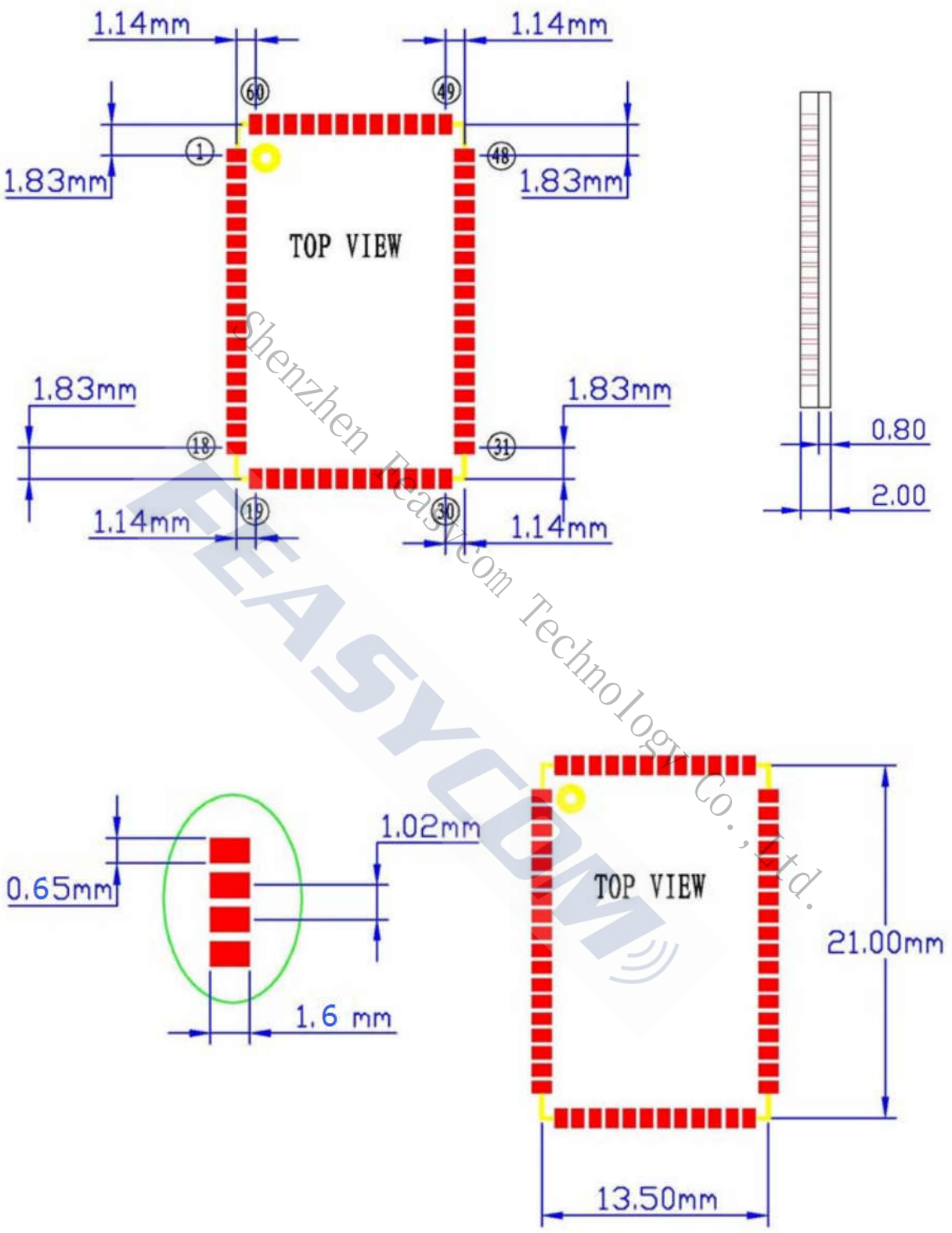

Figure 3: Footprint

3.2 Pin Description

Pin	Pin Name	Pad Type	Description
1	AIO1	Bi-directional	Programmable input/output line
2	AIO0	Bi-directional	Programmable input/output line
3	RESET	CMOS Input with weak internal pull-up	Reset if low. Input debounced so must be 5ms to cause a reset
4	GND	GND	Ground
5	PIO9	Bi-directional	Programmable input/output line Alternative function: PA_MUTE(Default)
6	PIO10	Bi-directional	Programmable input/output line
7	PIO11	Bi-directional	Programmable input/output line
8	PIO12	Bi-directional	Programmable input/output line
9	PIO13	Bi-directional	Programmable input/output line
10	PIO14	Bi-directional	Programmable input/output line
11	PIO15	Bi-directional	Programmable input/output line
12	GND	GND	Ground
13	VDD_IO	Power	+3.3V power supply
14	VDD_IO	Power	+3.3V power supply
15	1.8V_OUT	Power	+1.8V power output
16	GND	GND	Ground
17	USB_DP	Bi-directional	USB Date plus
18	USB_DN	Bi-directional	USB Date minus
19	UART_RTS	CMOS Output	UART Request to Send (active low)
20	UART_CTS	CMOS Input	UART Clear to Send (active low)
21	UART_RX	CMOS Input	UART Data input
22	UART_TX	CMOS Output	UART Data output
23	PCM_IN	CMOS Input	Synchronous data input
24	PCM_SYNC	Bi-directional	Synchronous data Sync
25	PCM_CLK	Bi-directional	Synchronous data clock
26	PCM_OUT	CMOS Output	Synchronous data output

27	SPI_CSB	CMOS input	Chip select for Synchronous Serial Interface, active low
28	SPI_MISO	CMOS output	Serial Peripheral Interface data output
29	SPI_CLK	CMOS input	Serial Peripheral Interface clock
30	SPI_MOSI	CMOS input	Serial Peripheral Interface data input
31	NC	NC	NC
32	VDD_3V3	Power	Lithium /polymer battery positive terminal. Battery charger output and input to switch-mode regulator
33	GND	GND	Ground
34	NC	NC	NC
35	LED1	Open drain output	LED driver
36	LED0	Open drain output	LED driver
37	GND	GND	Ground
38	SPK_L_N	Analogue	Speaker output negative , left
39	SPK_L_P	Analogue	Speaker output positive , left
40	SPK_R_N	Analogue	Speaker output negative , right
41	SPK_R_P	Analogue	Speaker output positive , right
42	GND	GND	Ground
43	MIC_BIAS	Analogue	Microphone bias
44	MIC_RP	Analogue	Microphone input positive , right
45	MIC_RN	Analogue	Microphone input negative , right
46	MIC_LP	Analogue	Microphone input positive , left
47	MIC_LN	Analogue	Microphone input negative , left
48	GND	GND	Ground
49	PIO0	Bi-directional	Programmable input/output line Alternative function: VOL+/NEXT(Default)
50	PIO1	Bi-directional	Programmable input/output line Alternative function: VOL-/BACK(Default)
51	PIO2	Bi-directional	Programmable input/output line Alternative function: PLAY/PAUSE(Default)
52	PIO3	Bi-directional	Programmable input/output line

53	GND	GND	Ground
54	RF	RF	RF Interface
55	GND	GND	Ground
56	PIO4	Bi-directional	Programmable input/output line
57	PIO5	Bi-directional	Programmable input/output line
58	PIO6	Bi-directional	Programmable input/output line, Alternative Function: I^2C Serial Clock input/output(Default)
59	PIO7	Bi-directional	Programmable input/output line, Alternative Function: I^2C Serial Data input/output(Default)
60	PIO8	Bi-directional	Programmable input/output line

Table 2: Pin Definition

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Audio Interfaces

Audio interface provides following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

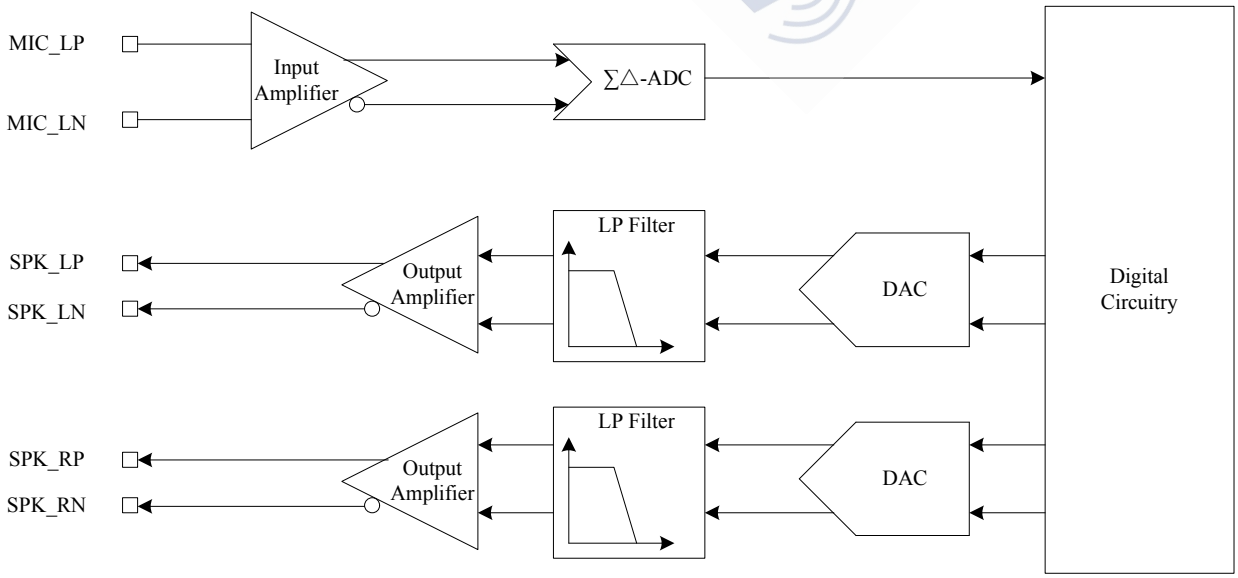

Figure 4: Audio Interface

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components. The module features a differential stereo audio output interfaces.

4.2.1 ADC

The ADC consists of a second order Digma Delta converter as show in Figure .

4.2.2 ADC Sample Rate Selection and Warping

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz.
One of the main concerns for stereo wireless music applications is the ability to keep sampling rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of 1/217, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

4.2.3 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

4.2.4 DAC

The DAC contains two second order Sigma Delta converters allowing two separate channels that are identical in functionality as show in Figure .

4.2.5 DAC Sample Rate Selection and Warping

Each DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz.
One of the main concerns for the DAC used in stereo wireless music applications is the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of 1/217, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

4.2.6 DAC Gain

The DAC contains two gain stages for each channel, a digital and an analogue gain stage.

4.2.7 Mono Operation

Mono operation is single channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxiliary mono channel that may be used in dual mono channel operation.

4.2.8 Audio Input Stage

The audio input stage of the module consists of a low noise input amplifier, which receives its analogue input signal from pins MIC_LP and MIC_LN to a second–order ∑-Δ ADC that outputs a 4Mbit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

4.2.9 Microphone Input

Check the Application Schematic for the microphone input design.

4.2.10 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.
The output circuit comprises a digital to analogue converter with gain setting and output amplifier. Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk-differential into a load of 16Ω. The output is available as a differential signal between SPK_LP and SPK_LN for the left channel; and between SPK_RP and SPK_RN for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.
The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.
The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

4.3 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via a software configured watchdog timer.
The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.
At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.4 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

4.5 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.6 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

4.7 Serial Interfaces

4.7.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators..

Parameters		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per channel		8

Table 3: Possible UART Settings

When connecting the module to a host, please make sure to follow .

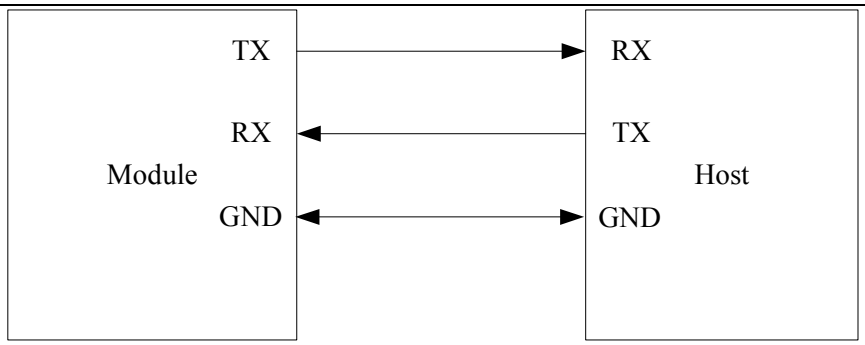

Figure 5: UART Connection

4.7.2 I²C Interface

PIO8, PIO7 and PIO6 can be used to form a master I²C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, Keyboard, scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2Kohm resistors.

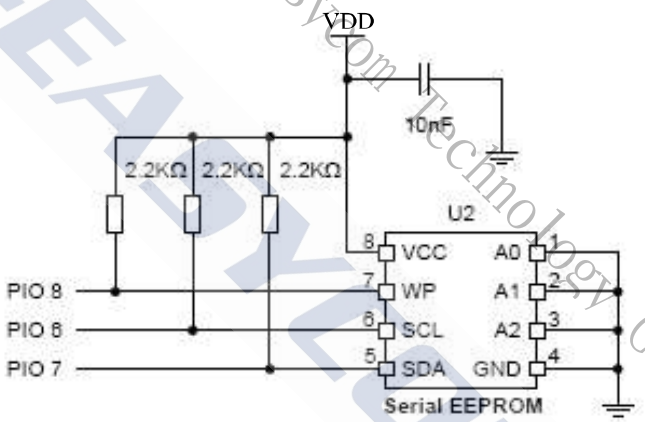

Figure 6: Example EEPROM Connection with I²C Interface

4.7.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

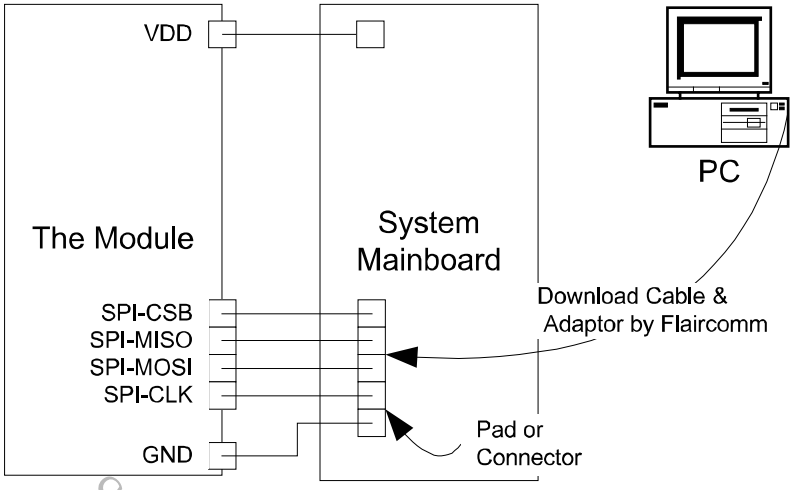

Figure 7: Design SPI for In-System Programming and Debug

4.7.4 USB

There is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.
The module features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD =3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and DP on the USB cable.

4.8 Digital Audio Interface(I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

The internal representation of audio samples within BlueCore5- Multimedia External is 16-bit and data on SD_OUT is limited to 16-bit per channel.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 4: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
PIO/AIO Voltage	-0.4	+3.6	V
VDD_IO,VDD_3V3 Voltage	-0.4	+3.6	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 5: Absolute Maximum Rating

5.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range (for A and I grade)	-40	--	+85	°C
Operating Temperature Range (for V and C grade)	-20	--	+70	°C
VDD_IO,VDD_3V3 Voltage	+2.7	+3.3	+3.6	V

Table 6: Recommended Operating Conditions

5.3 Input/output Terminal Characteristics

5.3.1 Input/output Terminal Characteristics

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.3	-	+0.25xVDD	V
VIH input logic level high	0.625VDD	-	VDD+0.3	V
Output Voltage Levels				
VOL output logic level low, IOL = 4.0mA	-	-	0.125	V
VOH output logic level high, IOH = -4.0mA	0.75xVDD	-	0.625xVDD	V
Input and Tri-state Current				

Ii input leakage current at Vin=VDD or 0V	-100	0	100	nA
Ioz tri-state output leakage current at Vo=VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	μA
With strong pull-down	10	40	100	μA
With weak pull-up	-5	-1.0	-0.2	μA
With weak pull-down	-0.2	+1.0	5.0	μA
I/O pad leakage current	-1	0	+1	μA
CI Input Capacitance	1.0	-	5.0	pF
Resistive Strength				
Rpuw weak pull-up strength at VDD-0.2V	500k	-	2M	Ω
Rpdw weak pull-up strength at 0.2V	500k	-	2M	Ω
Rpus strong pull-up strength at VDD-0.2V	10k	-	50k	Ω
Rpds strong pull-up strength at 0.2V	10k	-	50k	Ω

Table 7: Digital Terminal

5.3.2 USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
VIL input logic level low	-	-	0.3VDD	V
VIH input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < VIN < VDD(a)	-1	1	5	μA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
VIL output logic level low	0.0	-	0.2	V
VIH output logic level high	2.8	-	VDD	V

Table 8: USB Terminal

(a)Internal USB pull-up disabled

5.3.3 Internal CODEC - Analogue to Digital Converter

Parameter		Min	Typical	Max	Unit
Resolution		-	-	16	Bits
Input Sample Rate		8	-	44.1	kHz
Signal / Noise, fin=1kHz, BW=20Hz->20kHz A-Weighted THD+N<1% 150mV Vpk-pk					

Fsample = 8kHz		-	82	-	dB
Fsample = 11.025kHz		-	81	-	dB
Fsample = 16kHz		-	80	-	dB
Fsample = 22.05kHz		-	79	-	dB
Fsample = 32kHz		-	79	-	dB
Fsample = 44.1kHz		-	78	-	dB
Digital Gain		-24	-	21.5	dB

Table 9: Analogue to Digital Converter

5.3.4 Internal CODEC - Digital to Analogue Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Output Sample Rate, Fsample	8	-	48	kHz
Signal / Noise, fin=1kHz, BW=20Hz->20kHz A-Weighted THD+N<0.01% 0dBFS signal Load-100kΩ				
Fsample = 8kHz	-	95	-	dB
Fsample = 11.025kHz	-	95	-	dB
Fsample = 16kHz	-	95	-	dB
Fsample = 22.05kHz	-	95	-	dB
Fsample = 32kHz	-	95	-	dB
Fsample = 44kHz	-	95	-	dB
Fsample = 48kHz	-	95	-	dB
Digital Gain	-24	-	21.5	dB
Gain Resolution		1/32		dB

Table 1: Digital to Analogue Converter

5.3.5 Microphone Input

Microphone Input	Min	Typical	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain(differential)		800	-	mV rms
Gain	-3	-	42	dB
Gain resolution	-	3	-	dB
Distortion at 1kHz	-	-	-74	dB
3dB Bandwidth	-	20		kHz
Input impedance	-	6		kΩ
THD+N(microphone input)@30mV rms input	-	0.04	-	%

Table 2: Microphone Input

5.3.6 Speaker Output

Speaker Driver		Min	Typical	Max	Unit
Output voltage full scale swing (differential)		-	750	-	mV rms
THD+N 100kΩ load		-	-	0.01%	%
THD+N 16Ω load		-	-	0.1%	%
SNR(Load=16Ω, 0dBFS input relative to digital silence)		-	95	-	dB
Allowed Load	Resistive	16(8)	-	O.C.	Ω
	Capacitive	-	-	500	pF

Table 3: Microphone Output

5.4 Power consumptions

Search	Unconnected (Deep Sleep Idle Mode)	Connected Idle	Play with Minimum Volume	Play with Maximum Volume	Shutdown
~30mA	~0.57mA	~4mA	~40mA	~50mA	＜50uA

Table 4: Power consumptions

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

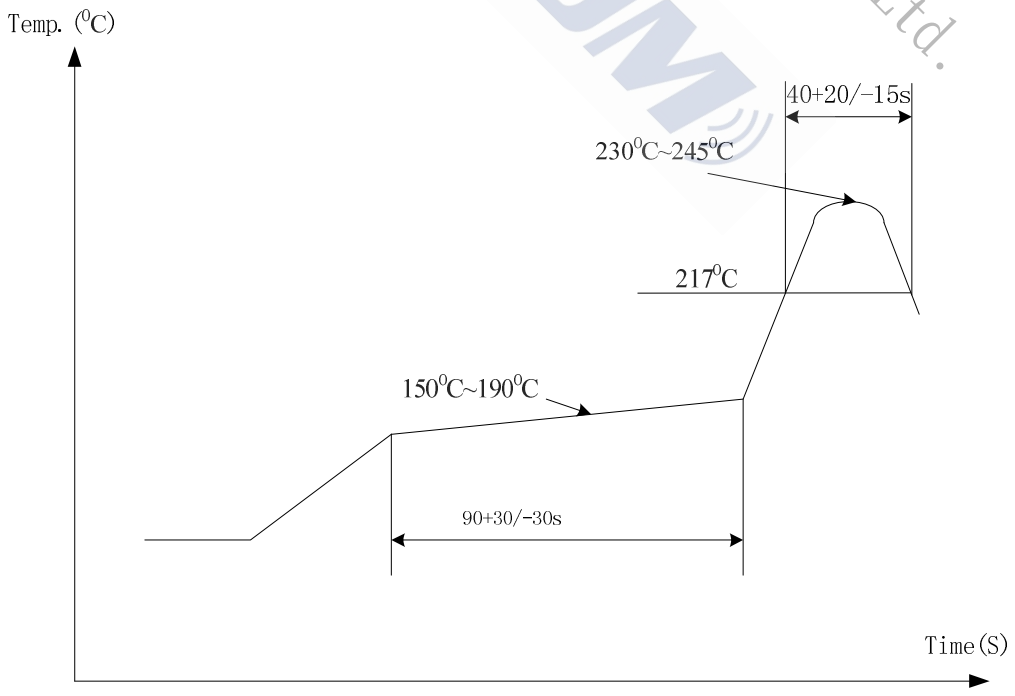

Figure 8 : Typical Lead-Free Re-flow Solder Profile

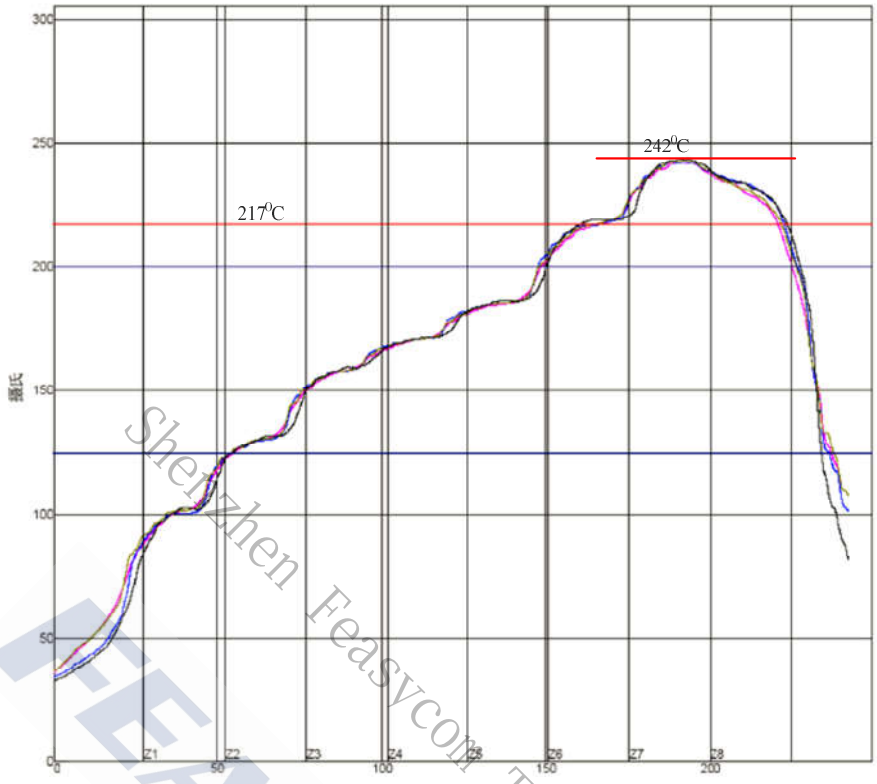

Figure 9: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow. FSC-BT502 will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －40℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －40℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation Test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop Test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging Information

After unpacking, the module should be stored in environment as follows:

- Temperature: 25℃ ± 2℃
- Humidity: <60%
- No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT502 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding via separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND via all around the PCB edges.

The mother board should have no bare conductors or via in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or via) are allowed in this area, because of mismatching the on-board antenna.

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground via around it. Locate them tightly and symmetrically around the signal via. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

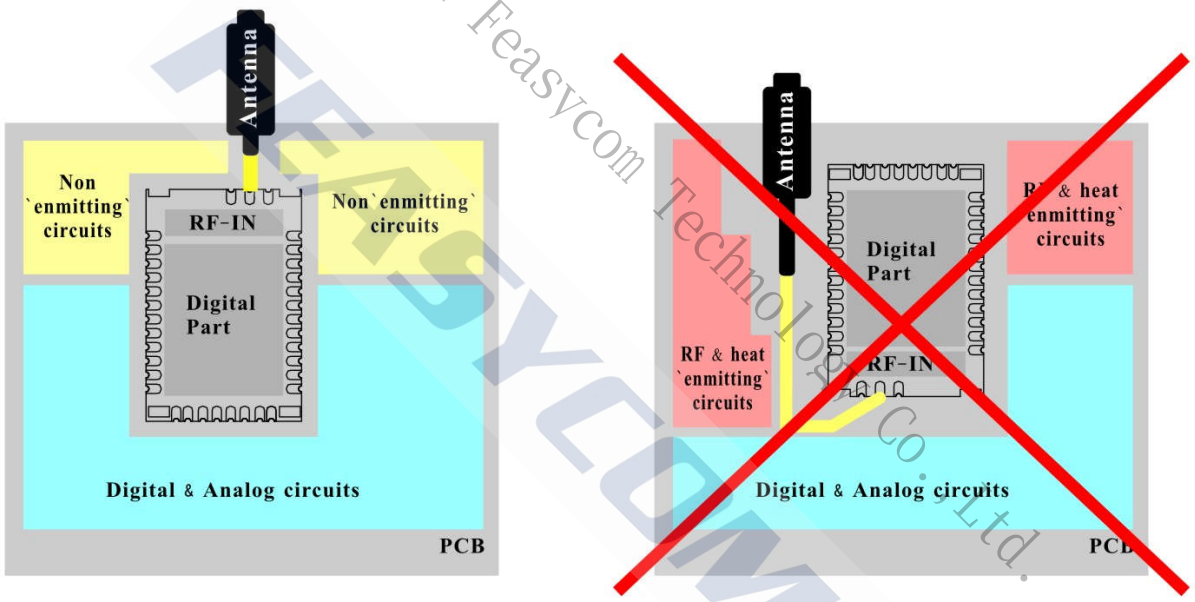

Figure 10: Placement the Module on a System Board

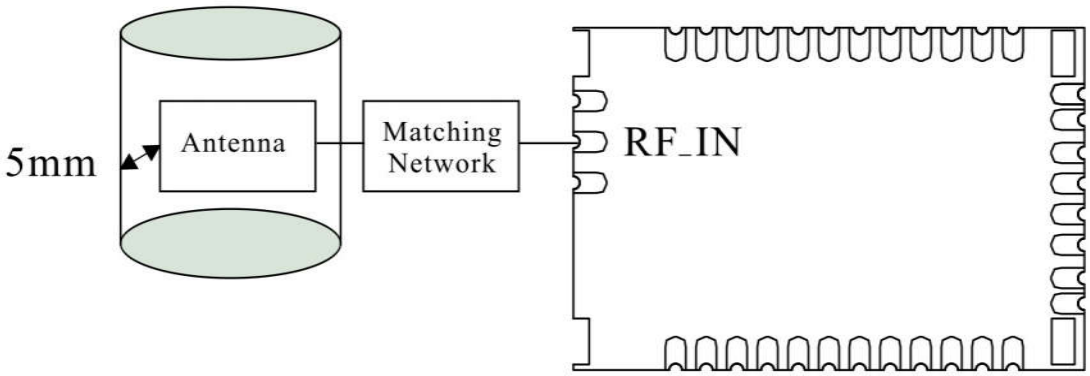

Figure 11: Leave 5mm Clearance Space from the Antenna

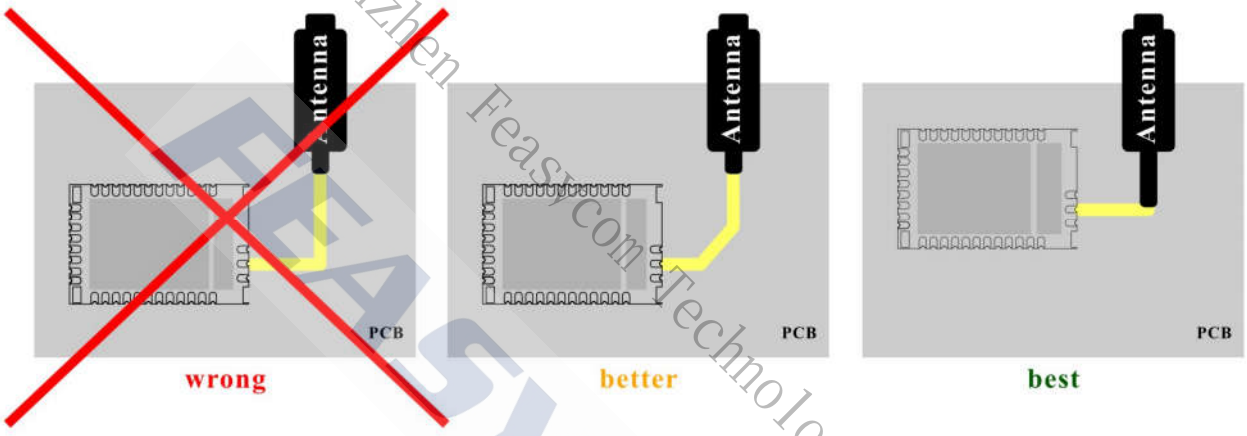

Figure 12: Recommended Trace Connects Antenna and the Module

9. Application Schematic