FSC-BT836

4.0 Dual Mode Bluetooth Module Data Sheet

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Shenzhen Feasycom Technology Co.,Ltd.

Telephone: 86-755-27924639

www.feasycom.com

Release Record

Version Number	Release Date	Comments
Revision 1.0	2016-04-18	First Release
Revision 1.1	2016-08-06	1, PIN27 Alternative Function :BT Power Mode 2, Modify the application circuit diagram.

1. INTRODUCTION

FSC-BT836 is a fully integrated Bluetooth module that complies with Bluetooth 4.0 dual mode protocols(BR/EDR/LE). It provides several interfaces such as UART, I^2C, PCM, AIO, PIO, USB etc., which can customized different applications.

FSC-BT836 supports various profiles. It integrates MCU, Baseband controller, RF, etc. in a small package, so the designers can have better flexibilities for the product shapes.

FSC-BT836 can be controlled by UART port or other interfaces. Please refer to Feasycom software design guide for the interfacing protocol.

1.1 Block Diagram

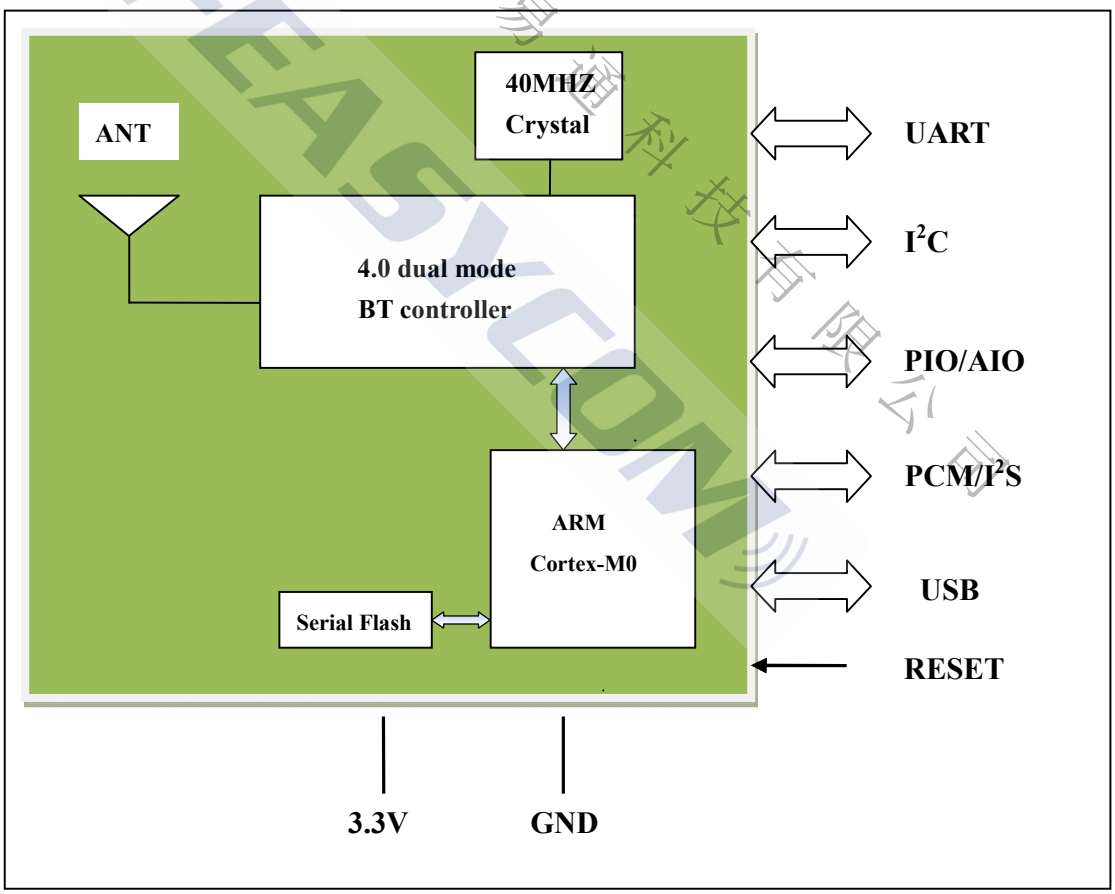


Figure 1

1.2 Feature

- Fully qualified Bluetooth 4.0/3.0/2.1/2.0/1.2/1.1
- Postage stamp sized form factor,
- Low power
- Class 1.5 support(high output power)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921Kbps,.
- UART, I^2C , PCM/I^2S ,USB data connection interfaces.
- Support the OTA upgrade.
- Embedded Bluetooth stack profiles support(requires no host stack): SPP, HID, MAP,and all BLE protocols.

1.3 Application

- Smart Watch and Bluetooth Bracelet
- Health & Medical devices
- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset tacking

2. GENERAL SPECIFICATION

General Specification	
Chip Set	Realtek RTL8761
Product ID	FSC-BT836
Dimension	13mm x 26.9mm x 2mm
Bluetooth Specification	Bluetooth V4.0 (Dual Mode)
Power Supply	3.3 Volt DC
Output Power	5.5 dBm (Class 1.5)
Sensitivity	-82dBm@0.1%BER
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	FHSS,GFSK,DPSK,DQPSK
Baseband Crystal OSC	40MHz
Hopping & channels	1600hops/sec, 1MHz channel space,79 Channels(BT 4.0 to 2MHz channel space)
RF Input Impedance	50 ohms
Antenna	Integrated chip antenna
Interface	Data: UART (Standard), I^2C Others: PIO, AIO, PWM.USB
Profile	SPP, GATT(BLE Standard) MFI, Airsync, ANCS, iBeacon, HID MAP(optional),OTA(optional)
Temperature	-20ºC to +70 ºC
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

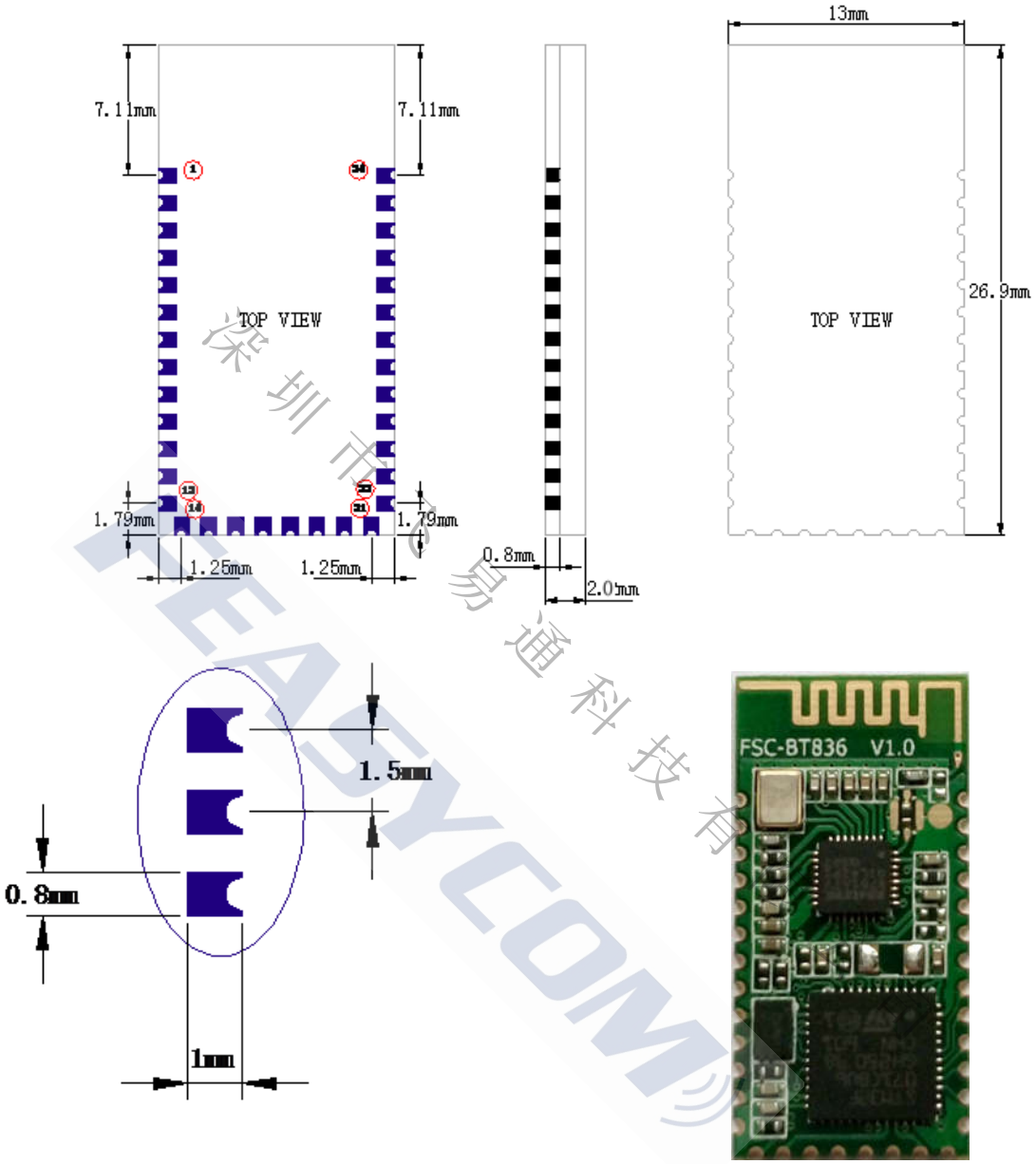


Figure 2

4. PIN DEFINITION DESCRIPTIONS

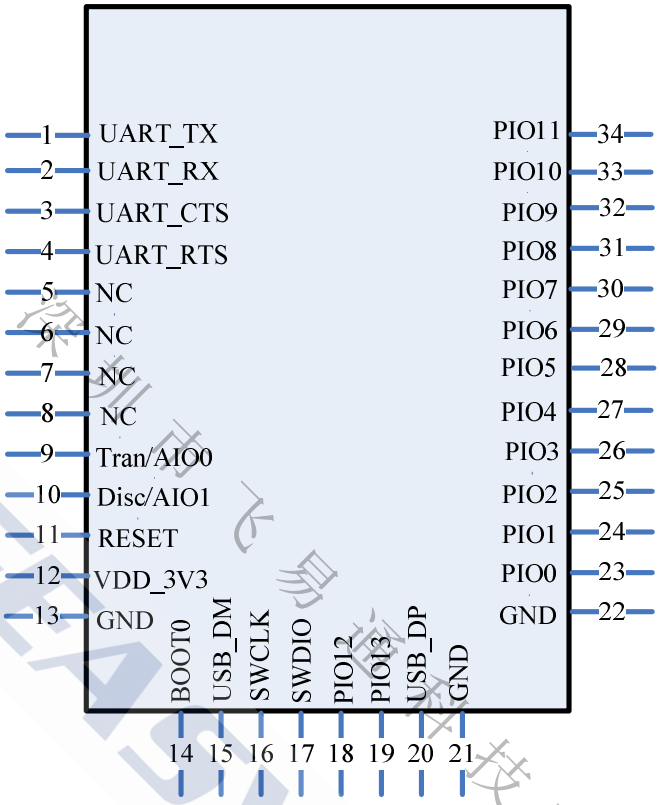


Figure 1: FSC-BT836 PIN Diagram

Pin NO.	Pin Name	Type	Pin Descriptions
1	UART_TX	CMOS output	UART data output
2	UART_RX	CMOS input	UART data input
3	UART_CTS	CMOS input	UART clear to send active low Alternative Function: Programmable input/output line
4	UART_RTS	CMOS output	UART request to send active low Alternative Function: Programmable input/output line
5	NC	NC	***Please have the pin dangling.***
6	NC	NC	***Please have the pin dangling.***
7	NC	NC	***Please have the pin dangling.***
8	NC	NC	***Please have the pin dangling.***

9	Tran/AIO0	I/O	Host MCU change UART transmission mode. (Default) If current UART transmission mode is command mode, one low pulse with 80ms duration low signal will change UART transmission mode to throughput mode, and another low pulse could change UART transmission mode back to command mode. Otherwise it will be set as high always. Alternative Function: Analogue programmable I/O line.
10	Disc/AIO1	I/O	Host MCU disconnect bluetooth. (Default) One low pulse with 80ms duration low signal to trigger bluetooth disconnection.Otherwise it will be set as high always. Alternative Function: Analogue programmable I/O line.
11	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
12	VDD_3V3	VDD	Power supply voltage 3.3V
13	GND	VSS	Power Ground
14	BOOT0	CMOS input	The default is low. (internal 10K resistance drop) When writing to MCU when using the serial port, this pin is connected with the high level.
15	USB_DM	Bi-directional	***USB_DM(optional)***
16	SWCLK	Bi-directional	Debugging through the clk line(Default)
17	SWDIO	Bi-directional	Debugging through the data line(Default)
18	PIO12	Bi-directional	Programmable input/output line ***Alternative Function: UART3 data output***
19	PIO13	Bi-directional	Programmable input/output line ***Alternative Function: UART3 data input***
20	USB_DP	Bi-directional	***USB_DP(optional)***
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	PIO0	Bi-directional	Programmable input/output line
24	PIO1	Bi-directional	Programmable input/output line
25	PIO2	Bi-directional	Programmable input/output line
26	PIO3	Bi-directional	Programmable input/output line

27	PIO4	Bi-directional	Programmable input/output line Alternative Function: BT Power Mode, low level in run mode, it will be set to high level when fall asleep.
28	PIO5	Bi-directional	Programmable input/output line
29	PIO6	Bi-directional	Programmable input/output line Alternative Function: I^2C Serial Clock input/output
30	PIO7	Bi-directional	Programmable input/output line Alternative Function:I^2C Serial Data input/output
31	PIO8	Bi-directional	Programmable input/output line
32	PIO9	Bi-directional	Programmable input/output line Alternative Function: LED(Default)
33	PIO10	Bi-directional	Programmable input/output line Alternative Function: BT Status(Default)
34	PIO11	Bi-directional	Programmable input/output line

Table 2

5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT836 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT836 module	Data from FSC-BT836 module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT836 module	Request to send output of FSC-BT836 module
UART-CTS	Host	Clear to send input of FSC-BT836 module

Table 3

Possible UART Settings

Property	Possible Values
BCSP-Specific Hardware	Enable or Disable
Baudrate	1200bps to 921Kbps
Flow Control	RTS/CTS or None
Data bit length	8bits
Parity	None, Odd or Even
Number of Stop Bits	1 or 2

Table 4

Default Data Format

Property	Possible Values
Baudrate	115.2Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 5

5.2 SPI /I^{2}S Interface

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I^{2}S interfaces supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

5.2.1 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$ (2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$ (3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

Table 6 SPI characteristics

1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

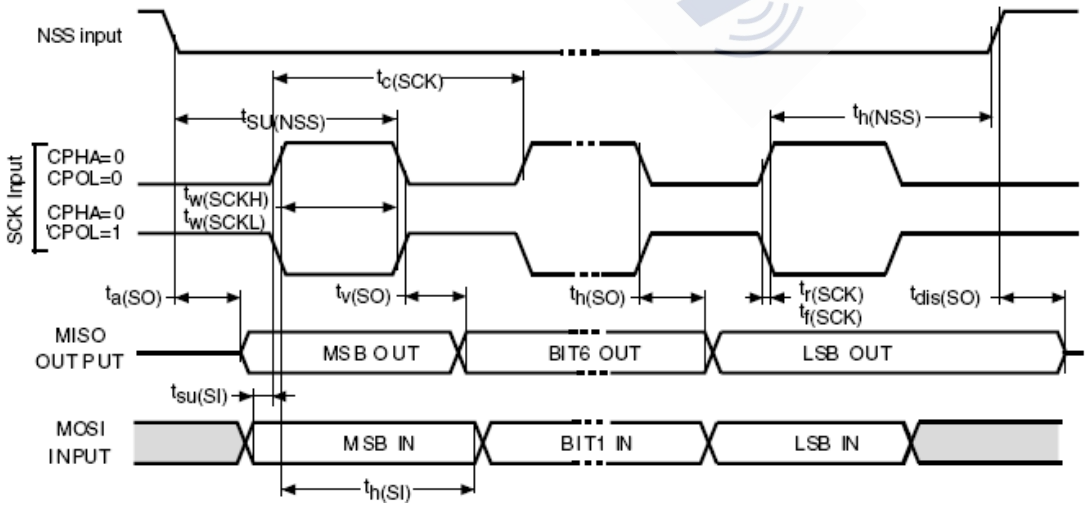
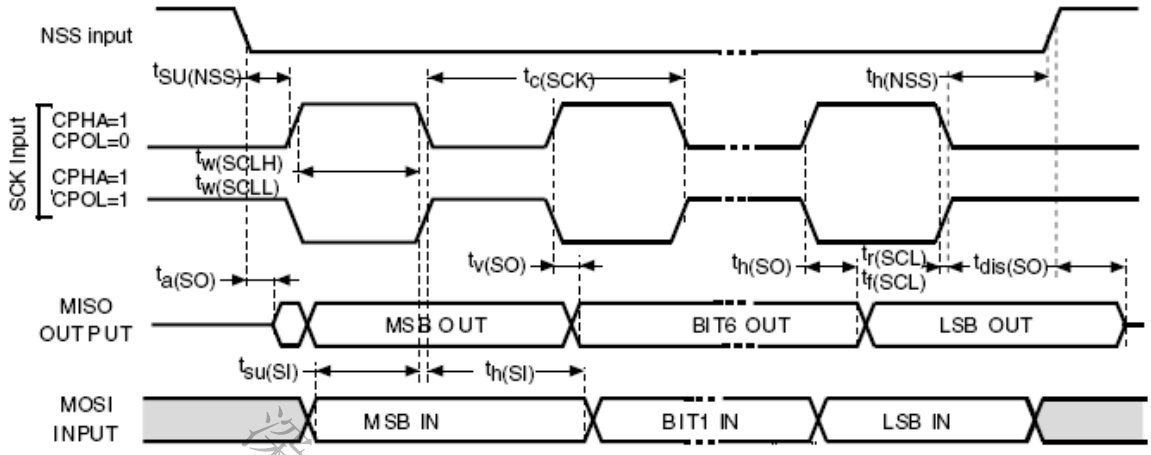
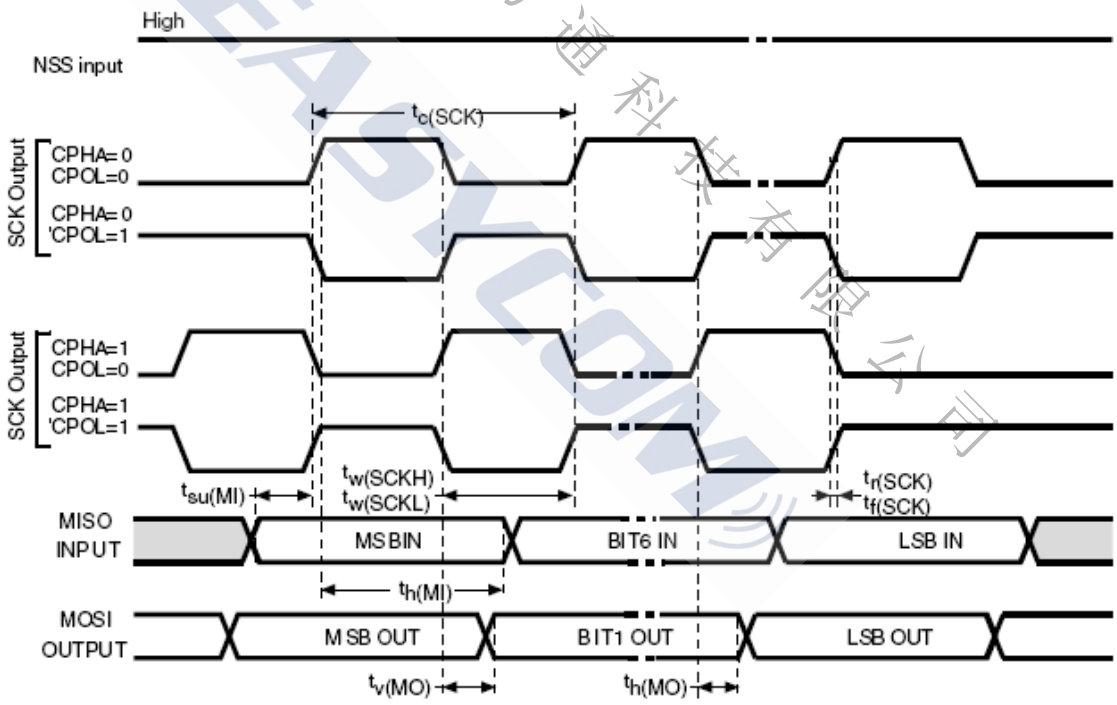


Figure 3: SPI timing diagram - slave mode and CPHA = 0



* 1. Measurement points are done at CMOS levels: 0.3 VDDand 0.7 VDD.

Figure 4: SPI timing diagram - slave mode and CPHA = 1



1.Measurement points are done at CMOS levels: 0.3 VDD and 0.7 VDD

Figure 5: SPI timing diagram - master mode

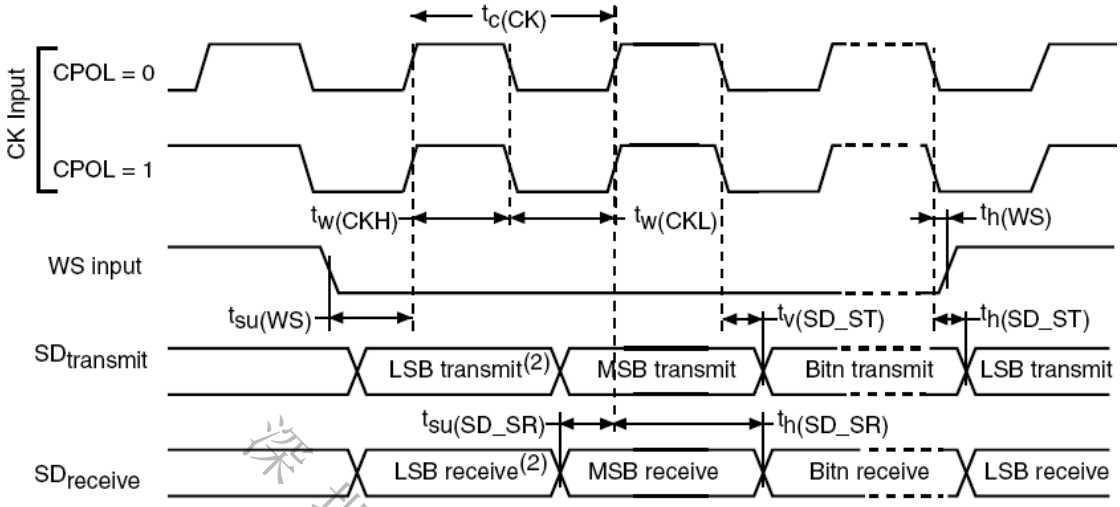
5.2.2 I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	%

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD\_MR)}$ (2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$ (2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$ (2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_{v(SD\_MT)}$ (2)	Data output valid time	Master transmitter (after enable edge)	-	4	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

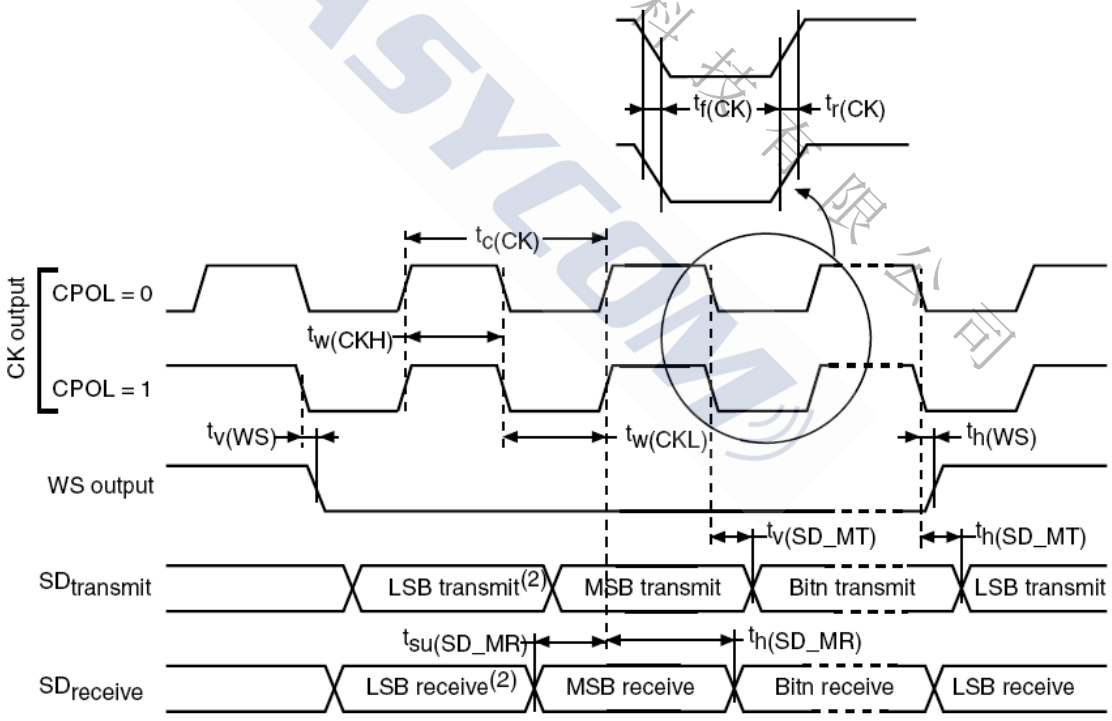
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on fPCLK. For example, if fPCLK = 8 MHz, then TPCLK = 1/fPLCLK = 125 ns.

Table 7 I^2S characteristics



1. Measurement points are done at CMOS levels: 0.3 × VDDIOx and 0.7 × VDDIOx.
2. LSB transmit/receive of the previously transmitted byte.
   No LSB transmit/receive is sent before the first byte.

Figure 6: I²S slave timing diagram (Philips protocol)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte.
   No LSB transmit/receive is sent before the first byte.

Figure 7: I²S master timing diagram (Philips protocol)

5.3 AIO , PIO lines I²C and USB

Up to 19 programmable bidirectional input/output (I/O) can be used.
Two general purpose analogue interface pin can be used.
PIO6 and PIO7 can be used as I²C interface.

Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

Universal serial bus (USB)

The FSC-BT836 embeds a full-speed USB device peripheral compliant with the USBspecification version 2.0.
The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support.

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 4 and Figure 5 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max
  - Cycloe interval：5 minus

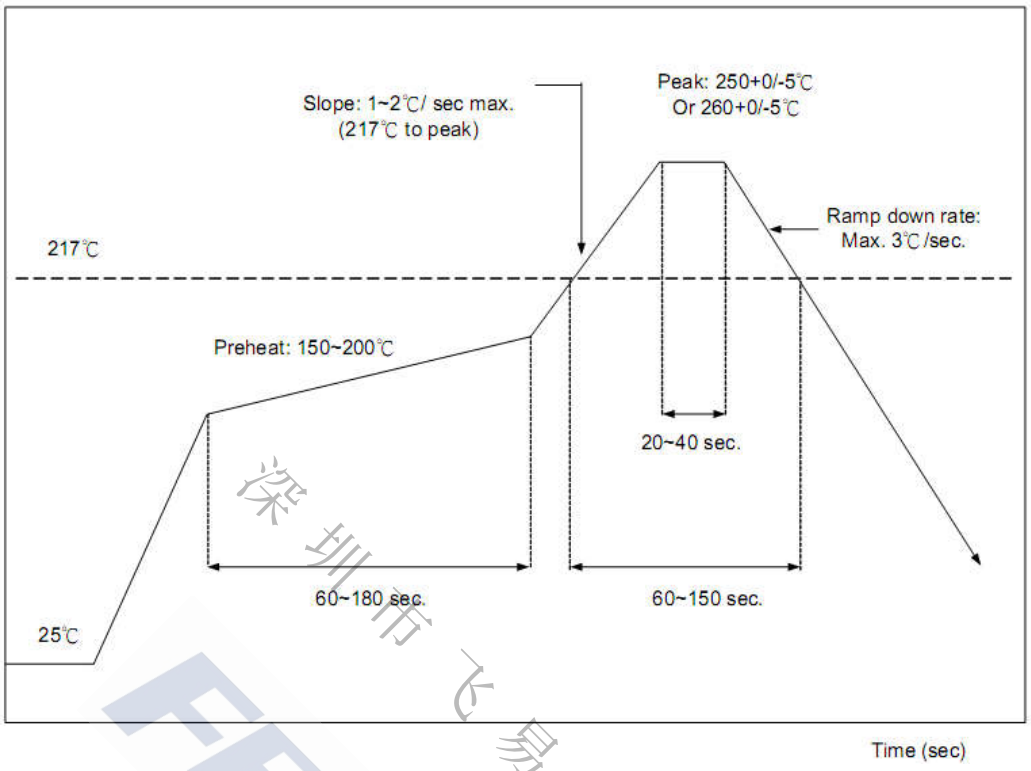


Figure 8: Typical Lead-free Re-flow Solder Profile

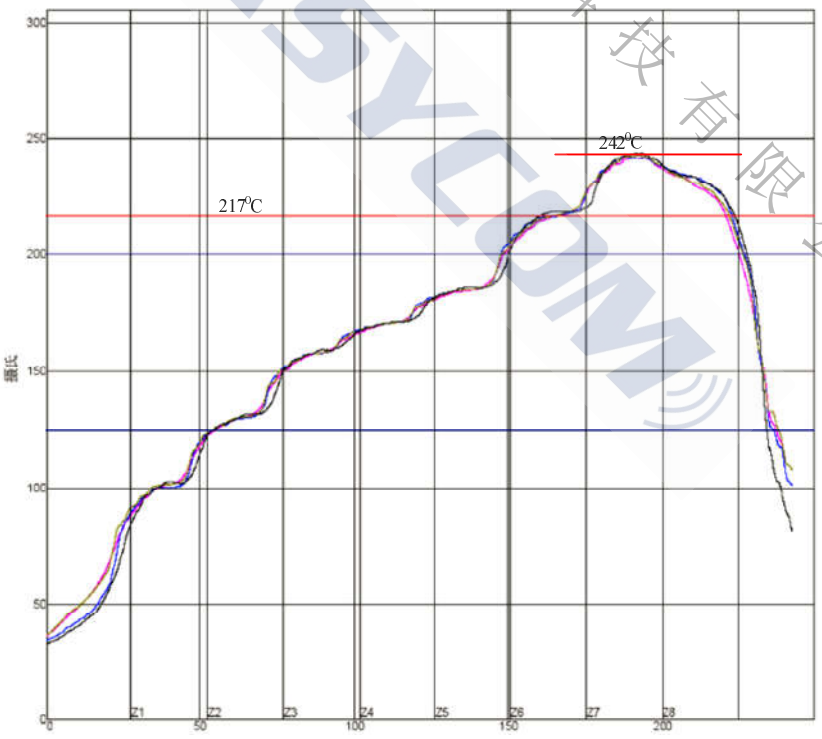


Figure 9: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT836 will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －40℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －40℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT836 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

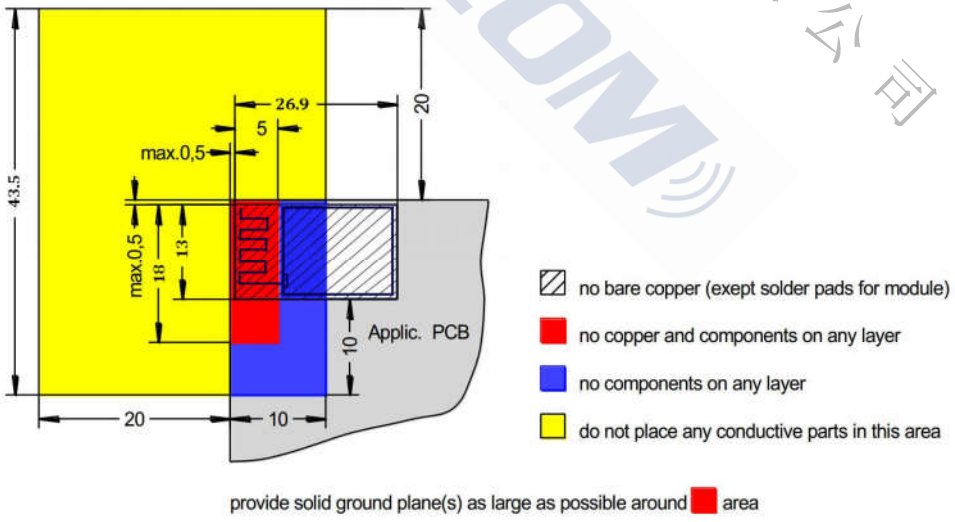


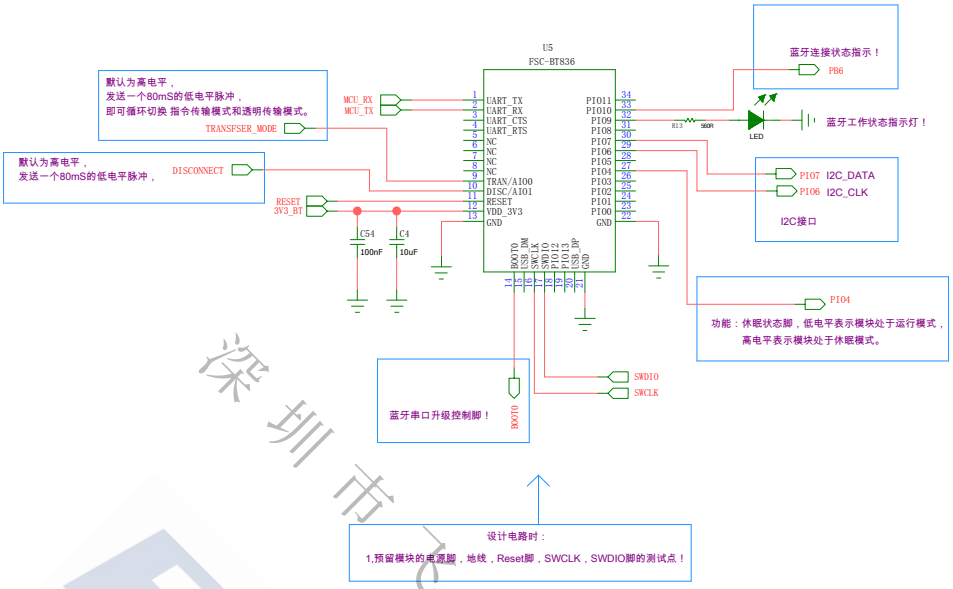
Figure 6: FSC-BT836 Restricted Area

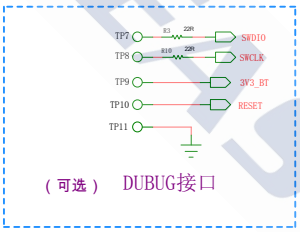
Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC

problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

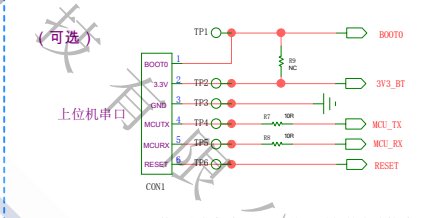
Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9. Application Schematic





	BOOT0
Serial Programming-Mode	1(接3.3V电源)
Run-Mode	0(模块内部已经有下拉电阻)



使用上位机串口对MCU烧录时候的电路接法

如果要实现不断电升级，

那么在升级完成后，需要对RESET脚复位操作一次。