FSC-BT803

CSR 8670 Bluetooth Module Data Sheet

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Revision History

Version	Date	Description
V1.0	2013-09-06	First Release
V1.3	2013-10-21	
V1.6	2015-09-11	
V1.7	2016-01-21	1 Modify the pin definition 2 Increase the application circuit diagram
V1.8	2016-04-22	1 Modify the pin definition 2 Modify the application circuit diagram.

1. INTRODUCTION

The FSC-BT803 Bluetooth® module is a perfect 4.0 dual-mode solution for wireless applications, such as smart watches, Bluetooth Bracelets, and wireless transmission devices. It can be connected with any Bluetooth® devices in an operating range. It is small and thin so the designers can have better flexibilities for the product shapes.

The FSC-BT803 Bluetooth® module complies with Bluetooth® specification version 4.0. It supports HSP,HFP,A2DP,AVRCP,PBAP,MAP,SPP, BLE,etc profiles. It integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, LED and LCD drivers in a SOC IC. The dual-core architecture with flash memory enables manufactures to easily differentiate their products with new features without extending development cycles. It integrates RF Baseband controller, (Need an external RF antenna),etc. and provide UART interface, programmable I/O, stereo speaker output, microphone input,etc.

The detail information of FSC-BT803 Bluetooth® module is presented in this document below.

1.1 Block Diagram

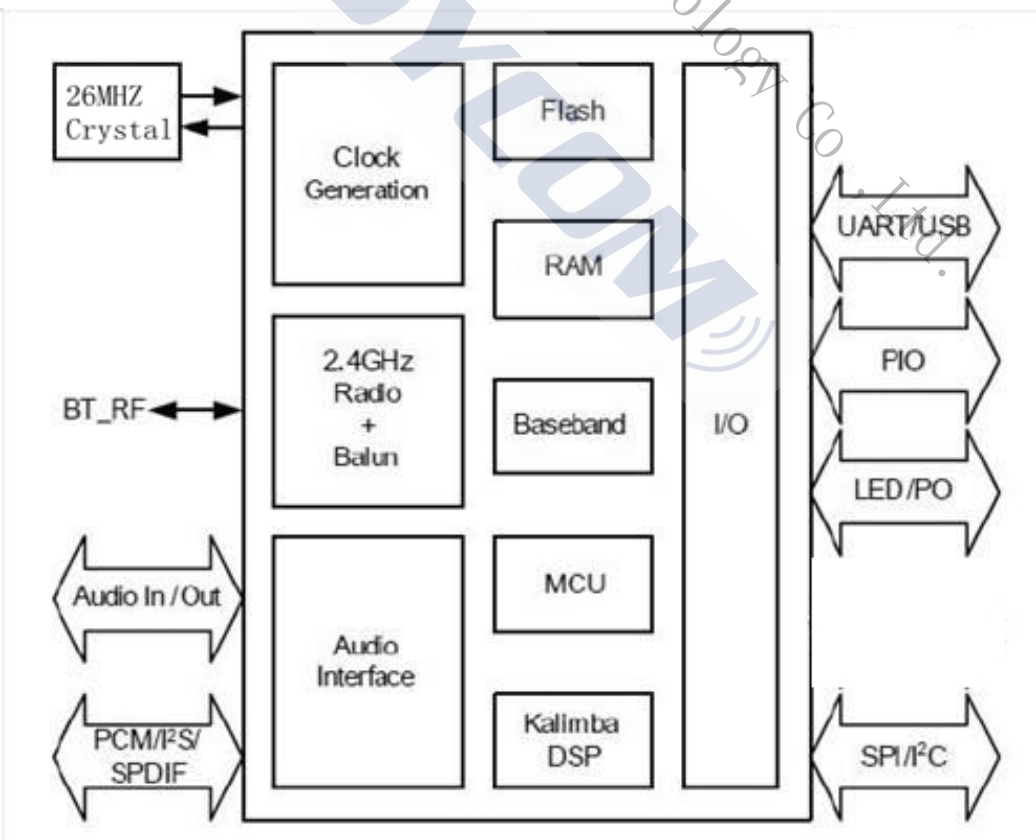

Figure 1

1.2 Features

- ✓ Small overall dimension
- ✓ Bluetooth Specification V4.0(Dual Mode)
- ✓ Class1,Class 2 and Class 3 support
- ✓ Physical connection as SMD type
- ✓ 80MHz RISC MCU and 80MIPS Kalimba DSP
- ✓ 16Mb internal flash memory(64-bit wide,45ns); optional support for 64Mb of external SPI flash
- ✓ Stereo codec with 1 channels ADC and 1 microphone inputs
- ✓ Support I^2S interface
- ✓ Support for CSR's latest CVC technology for narrow-band and wideband voice connections including wind noise reduction
- ✓ Music Enhancements: SBC,MP3,AAC and AAC+,Faststream codec,atpX,5-band EQ,3D stereo separation and so on.
- ✓ Serial Interfaces: UART,USB 2.0,I^2C and SPI
- ✓ Support HSP, HFP, A2DP, AVRCP,PBAP,MAP,SPP,BLE profile
- ✓ Multipoint support for HFP connection to 2 handsets for voice
- ✓ Multipoint support for A2DP connection to 2 A2DP source for music playback
- ✓ 2 Hardware LED controllers and ability to drive LCD segment display directly
- ✓ Support for up to 6 capacitive touch sensor inputs(optional)
- ✓ Built-in RF combo filter, Integrated 26M Crystal.
- ✓ No radio signal interference, support for 802.11 co-existence

※ ***Some features are optional for customization on demand.***

1.3 Application

- ✓ Smart watches
- ✓ Bluetooth bracelets
- ✓ Bluetooth headphones
- ✓ Smart remote controllers
- ✓ Wired or wireless sound bars
- ✓ Wired or wireless speakers
- ✓ Wearable audio with sensors(health and well-being applications)

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chipset	CSR8670
Module	FSC-BT803
Dimension	13mm x 13mm x 2.0mm
BT Standard	Bluetooth® V4.0 specification
RF TX Output Power	10dBm (Max)
Sensitivity	-85dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	26MHz
Hopping	1600hops/sec, 1MHz channel space (BT 4.0 to 2MHz channel space)
RF Input Impedance	50 ohms
Major Interface	• Microphone : Input (Differential) • Speaker : Output (Differential) • UART : Tx/Rx • AIO/PIOs • PCM/I2S • USB • Antenna
Profile	HSP, HFP, A2DP, AVRCP,PBAP,MAP,SPP, GATT(BLE Standard)
Voice Processor	80MIPS Kalimba with cVc support
Power	
Supply Voltage	VBAT=4.2V MAX ; 3V3_INPUT=1.7~3.6V Volt DC
Working Current	Depends on profiles
Standby Current	<1mA
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

3.1 Physical Dimensions

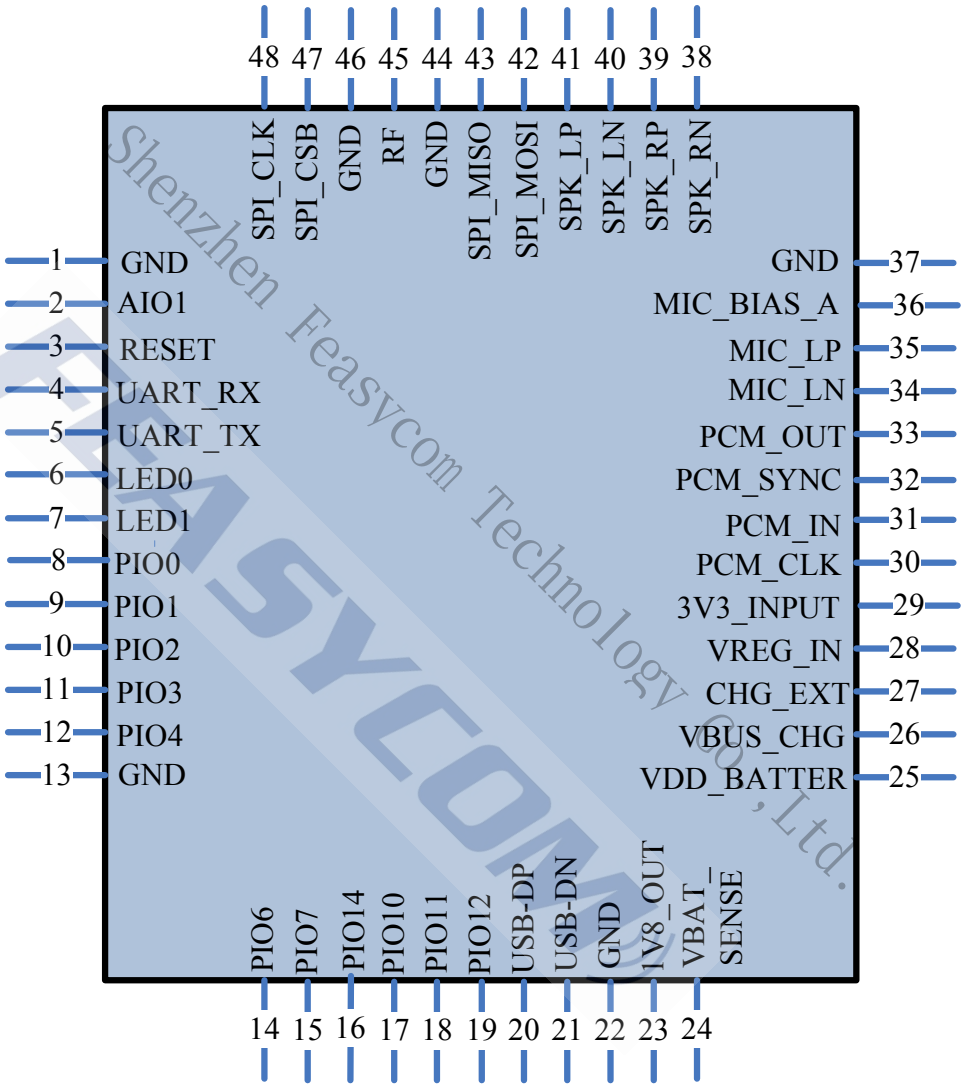

Figure 2 PIN Diagram

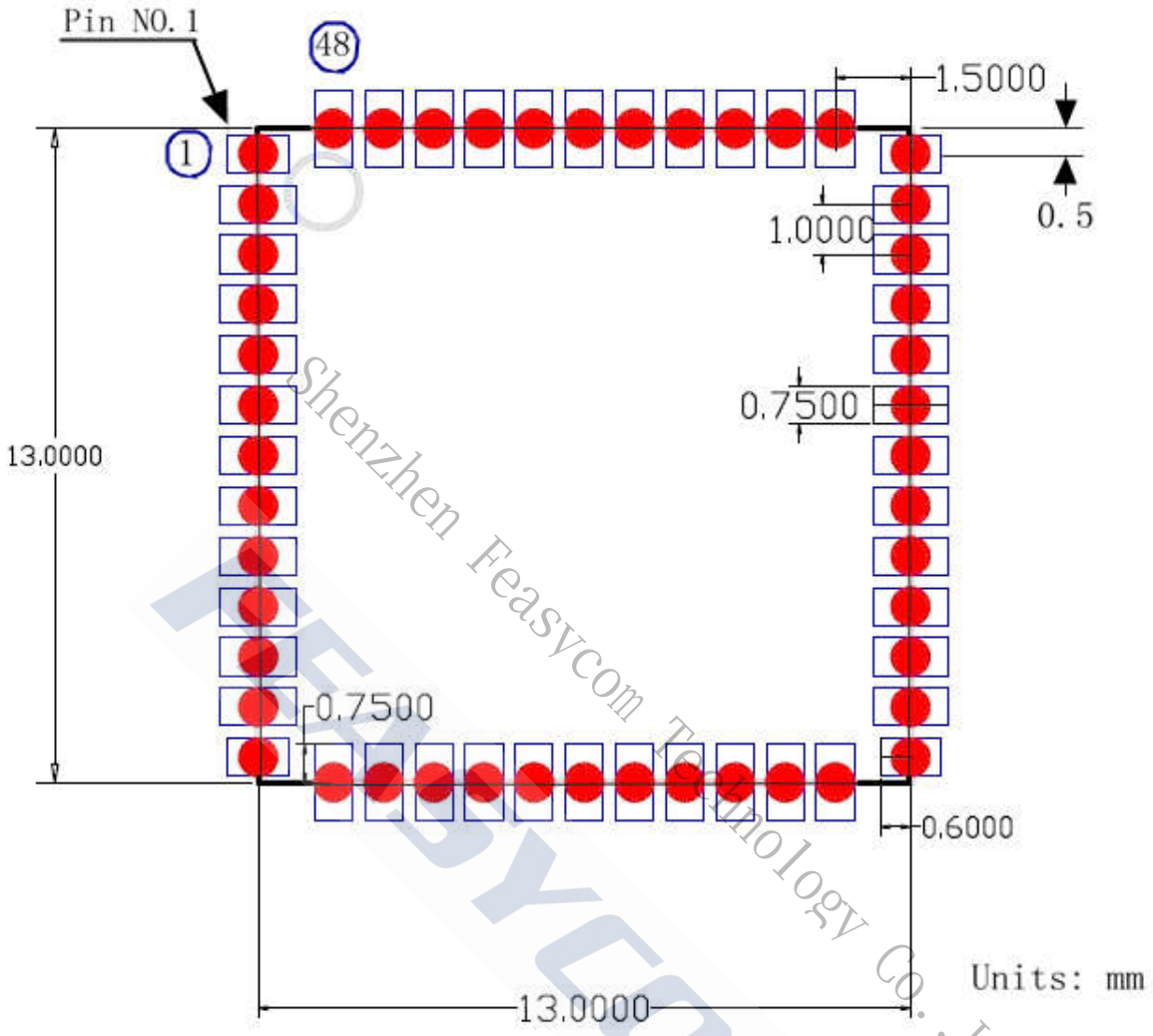

Figure 3 Footprint

3.2 Pin Description

Pin	Pin Name	Pad Type	Description
1	GND	VSS	Power Ground
2	AIO1	Bi-directional	Analogue programmable input / output line
3	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
4	UART_RX	CMOS input	UART data input
5	UART_TX	CMOS output	UART data output
6	LED0	Open drain	LED driver(Default) Alternative function: PIO[29]
7	LED1	Open drain	LED driver(Default) Alternative function: PIO[30]
8	PIO0	Bi-directional	Programmable input/output line Alternative function: VOL+/NEXT(Default)
9	PIO1	Bi-directional	Programmable input/output line Alternative function: VOL-/BACK(Default)
10	PIO2	Bi-directional	Programmable input/output line Alternative function: PLAY/PAUSE(Default)
11	PIO3	Bi-directional	Programmable input/output line Alternative function: BT Status(Default)
12	PIO4	Bi-directional	Programmable input/output line Alternative function: PA_MUTE(Default)
13	GND	VSS	Power Ground
14	PIO6	Bi-directional	Programmable input/output line, Alternative Function: I^2C Serial Clock input/output(Default)
15	PIO7	Bi-directional	Programmable input/output line, Alternative Function: I^2C Serial Data input/output(Default)
16	PIO14	Bi-directional	Host MCU disconnect bluetooth. (Default) One low pulse with 80ms duration low signal to trigger bluetooth disconnection.Otherwise it will be set as high always. Alternative Function: Programmable input/output line,
17	PIO10	Bi-directional	Host MCU change UART transmission mode. (Default) If current UART transmission mode is command mode, one low pulse with 80ms duration low signal will change UART transmission mode to throughput mode, and another low pulse could change UART transmission mode back to command mode.

			Otherwise it will be set as high always. Alternative Function: Programmable input/output line.
18	PIO11	Bi-directional	Programmable input/output line
19	PIO12	Bi-directional	Programmable input/output line
20	USB_DP	I/O	USB data plus with selectable internal 1.5kohm pull-up resistor
21	USB_DN	I/O	USB data minus
22	GND	VSS	Power Ground
23	1V8_OUT	Open drain output	+1V8 OUT
24	VBAT_SENSE	Battery charger sense	Battery charger sense input
25	VDD_BATTER	Battery	Battery positive terminal
26	VBUS_CHG	Charger	Battery charger input
27	CHG_EXT	External charger	Lithium ion/polymer battery charger input
28	VREG_IN	Input enable	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input. *** The PIN on electricity than VBAT foot 100 ms delay.**
29	3V3_INPUT	Connect to 3.3V	1.7V to 3.6V positive supply input for digital input/output ports
30	PCM_CLK	Synchronous	PCM data clock
31	PCM_IN	Synchronous	PCM data input
32	PCM_SYNC	Synchronous	PCM data sync
33	PCM_OUT	Synchronous	PCM data output
34	MIC_LN	Analogue in	Microphone input negative, left
35	MIC_LP	Analogue in	Microphone input positive, left
36	MIC_BIAS_A	Analogue out	Microphone bias A
37	GND	VSS	Power Ground
38	SPKR_RN	Analogue out	Speaker output negative, right
39	SPKR_RP	Analogue out	Speaker output positive, right
40	SPKL_LN	Analogue out	Speaker output negative, left
41	SPKL_LP	Analogue out	Speaker output positive, left

42	SPI_MOSI	CMOS input with weak internal pull-down	Serial peripheral interface data input
43	SPI_MISO	CMOS input with weak internal pull-down	Serial peripheral interface data Output
44	GND	VSS	Power Ground
45	RF	RF_IN	Bluetooth 50ohm transmitter output/ receiver input
46	GND	VSS	Power Ground
47	SPI_CSB	CMOS input with weak internal pull-up	Chip select for serial peripheral interface, active low
48	SPI_CLK	CMOS input with weak internal pull-down	Serial peripheral interface clock

Table 2

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less.

4.2 Audio Interfaces

The Audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual analogue audio outputs
- 6 digital MEMS microphone inputs
- A configurable PCM, I²S or SPDIF interface

Figure shows the functional blocks of the interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.

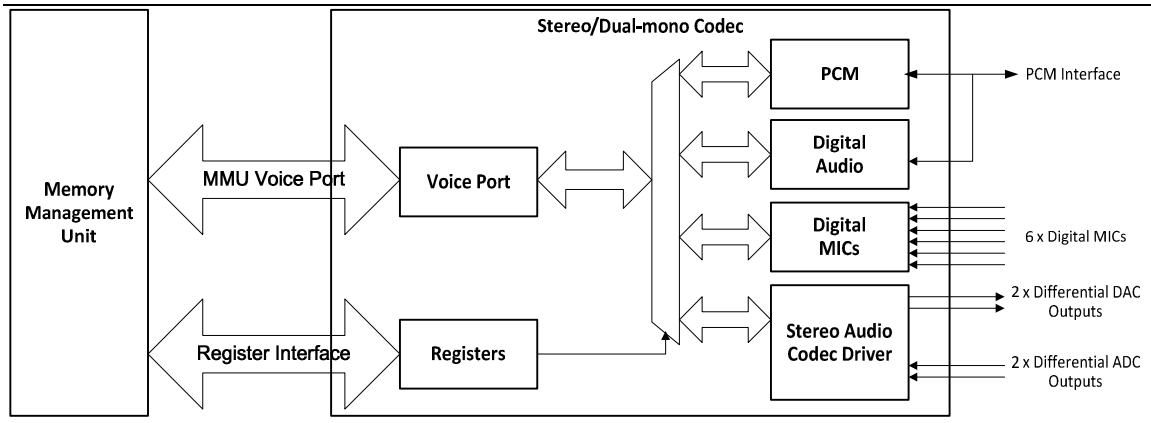

Figure 4 Audio Interface

The interface for the digital audio bus shares the same pins as the PCM CODEC interface, which means that each of the audio buses are mutually exclusive in their usage. These alternative functions are summarized in

Table below.

PCM Interface	SPDIF Interface	I2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Table 3 Alternative functions of the digital audio bus interface on the PCM interface

4.2.1 Audio Input and Output

The audio input circuitry consists of:

- 2 independent 16-bit high-quality ADC channels:
  - Programmable as either microphone or line input
  - Programmable as either stereo or dual-mono inputs
  - Multiplexed with 2 of the digital microphone inputs
  - Each channel is independently configurable to be either single-ended or fully differential
  - Each channel has an analogue and digital programmable gain stage for optimisation of different microphones
- 6 digital MEMS microphone channels, of which 4 have independent codec channels and 2 share their codecs with the 2 high-quality audio inputs

The audio output circuitry consists of a dual differential class A-B output stage.

4.2.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I²S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. SPDIF and AES3 (also known as AES/EBU)
- Support for PCM interfaces including PCM master codecs that require an external system clock

4.2.3 ADC

FSC-BT803 consists of 1 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

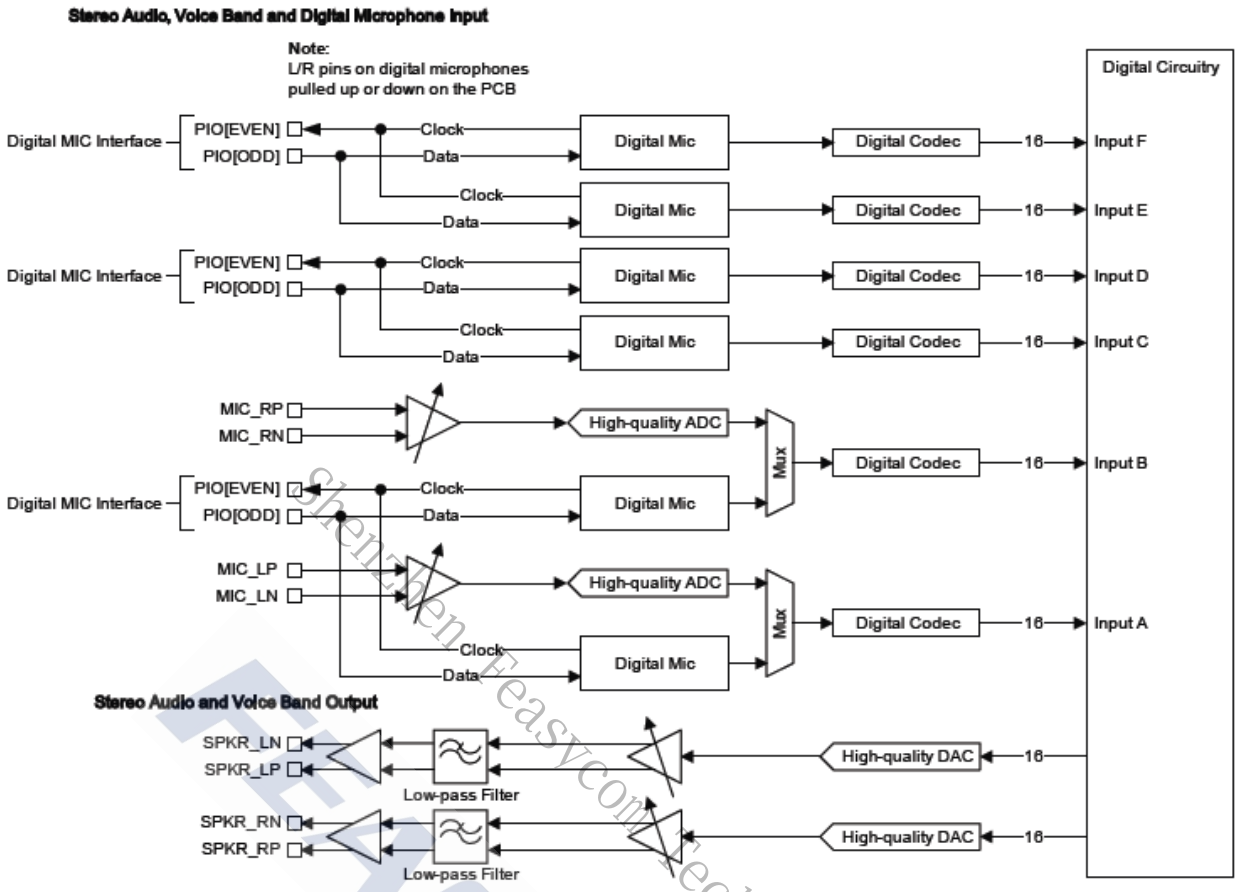

Figure 5 Audio Codec Input and Output Stages

4.2.3.1 ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are progrmmable,e.g.40kHz:

- 8kHz
- 11.025 kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32 kHz
- 44.1kHz
- 48 kHz

4.2.3.2 ADC Audio Input Gain

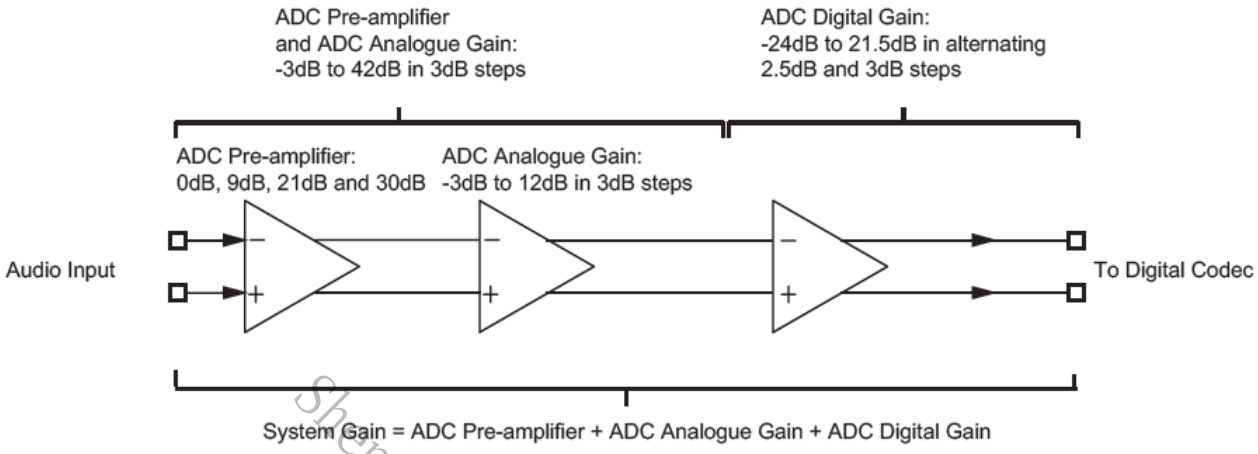

Figure 6 Audio Input Gain

4.2.3.3 ADC Pre-amplifier and ADC Analogue Gain

FSC-BT803 has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB
- The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps, see Figure above.
- At mid to high gain levels it acts as a microphone pre-amplifier,
  At low gain levels it acts as an audio line level amplifier

4.2.3.4 ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see Table . There is also a fine gain interface with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact Feasycom.

Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

. **Table 4** ADC Digital Gain Rate Selection

4.2.4 DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical functionality,as figure 4 shows
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

4.2.4.1 DAC Sample Rate Selection

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

4.2.4.2 DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB,see as below,there is another a fine gain interface with 9-bit gain setting enabling gain changes in 1/32 steps.
The overall gain control of the ADC is controlled by the firmware.Its setting is a combined function of the digital and analogue amplifier settings.

Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 5 DAC Digital Gain Rate Selection

4.2.4.3 DAC Analogue Gain

As below shows that the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps
The firmware controls the overall gain control of the DAC.Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Setting	DAC Gain Setting (dB)	Analogue Gain Setting	DAC Gain Setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

Table 1 DAC Analogue Gain Rate Selection

4.2.5 Microphone Input

FSC-BT803 contains 1 independent low-noise microphone bias generators.The microphone bias generators are recommended for biasing electret condensor microphones.A biasing circuit for microphones with a sensitivity between about -40dB to -60dB(0dB=1V/Pa)

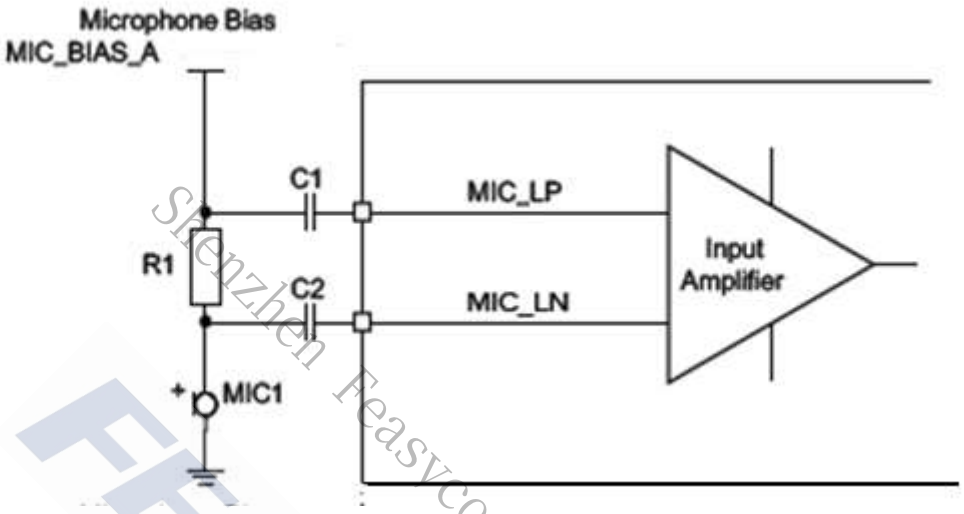

Figure 7 Microphone Biasing

4.2.6 Line Input

In this line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting.

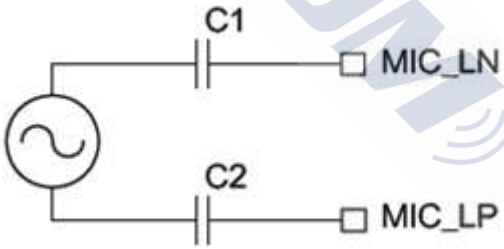

Figure 8 Differential Input

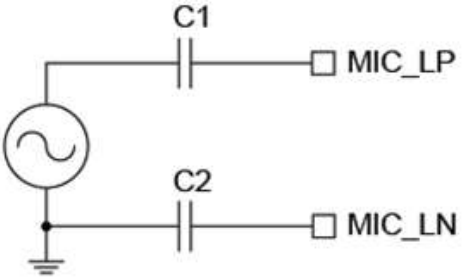

Figure 9 Single-ended Input

4.2.7 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.
The output circuit comprises a digital to analogue converter with gain setting and output amplifier.Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of 16Ω. The output is available as a differential signal between SPK_R_RP and SPK_R_RN for the left channel; and between SPK_L_LP and SPK_L_LN for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

- 13-bit or 16-bit linear,8-bit u-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 the first 4 slots following PCM_SYNC.

4.3 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

4.4 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.5 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

4.6 Serial Interfaces

4.6.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX

transfer data between the two devices.

Parameters		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per channel		8

Table 7 Possible UART Settings

4.6.2 I²C Interface

As this I²C interface is software-driven it is suited to relatively slow functions such as driving a dot matrix LCD, keyboard scanner or EEPROM. If it is not used, then PIO[7:6] are available to form a software-driven master I²C interface.

4.6.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

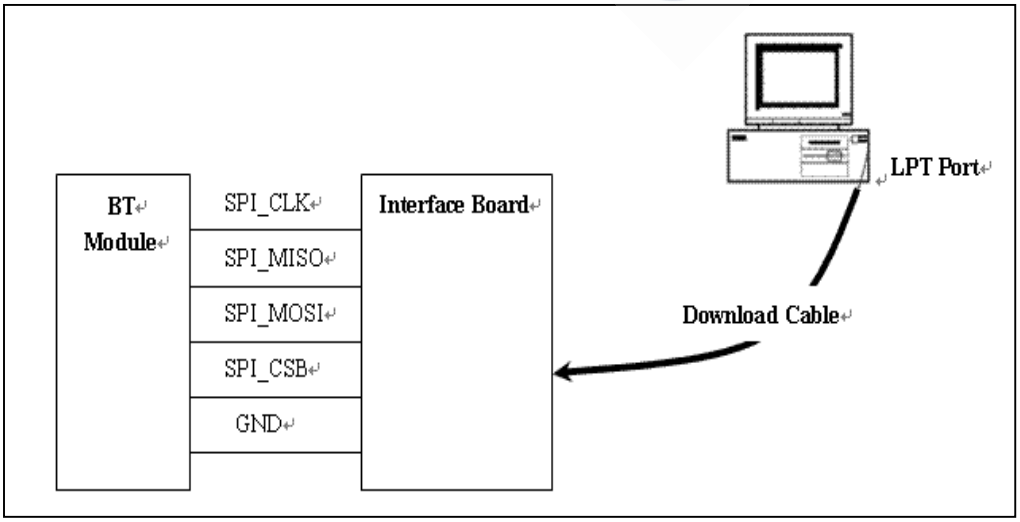

Figure 10

4.7 Digital Audio Interface(I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 8: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
Supply Voltage				
5V(USB VBUS)	CHG	-0.4	5.75	V
3.3V	3V3_INPUT	-0.4	3.60	V
Battery	LED[1:0]	-0.4	4.40	V
	VBAT	-0.4	4.40	V
	VBAT_SENSE	-0.4	4.40	V
	VREG_IN	-0.4	4.40	V
Other terminal voltages		VSS - 0.4	VDD + 0.4	V

Table 9

5.2 Recommended Operating Conditions

Rating		Min	Type	Max	Unit
Operating temperature range		-40	20	85	°C
Supply Voltage					
5V(USB VBUS)	CHG	4.75 / 3.10	5	5.75	V
Battery	LED[2:0]	1.1	3.7	4.25	V
	VBAT	0	3.7	4.25	V
	VBAT_SENSE	0	3.7	4.25	V
	VREGENABLE	0	3.7	4.25	V
3.3V	3V3_INPUT	1.7	3.3	3.6	V

Table 10

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

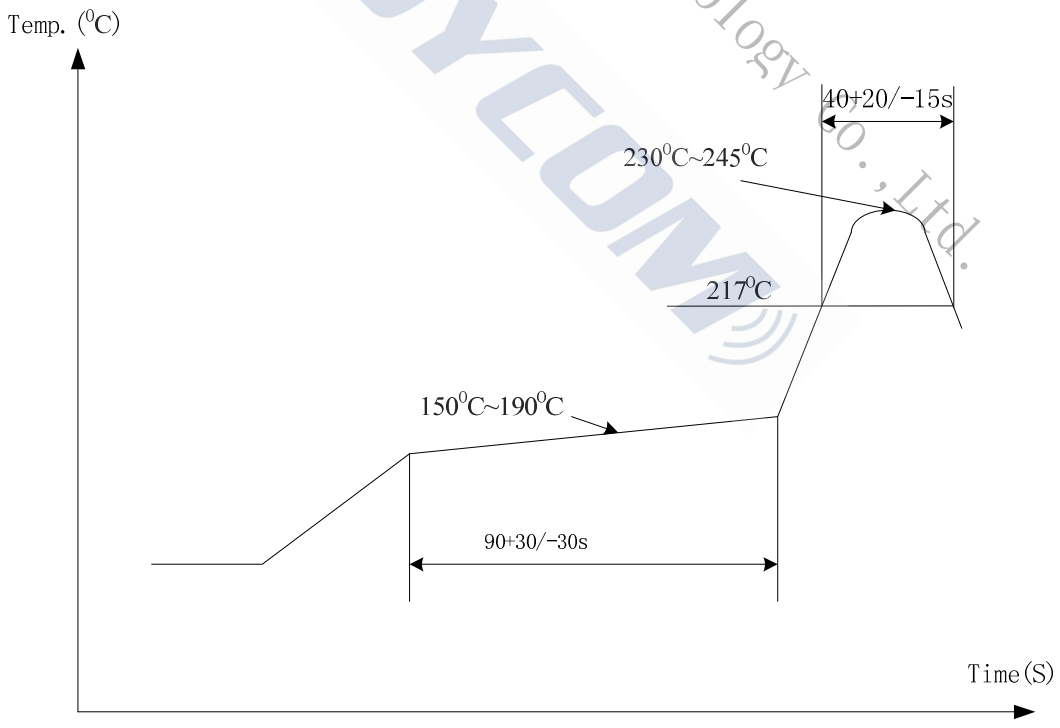

Figure 11 Typical Lead-Free Re-flow Solder Profile

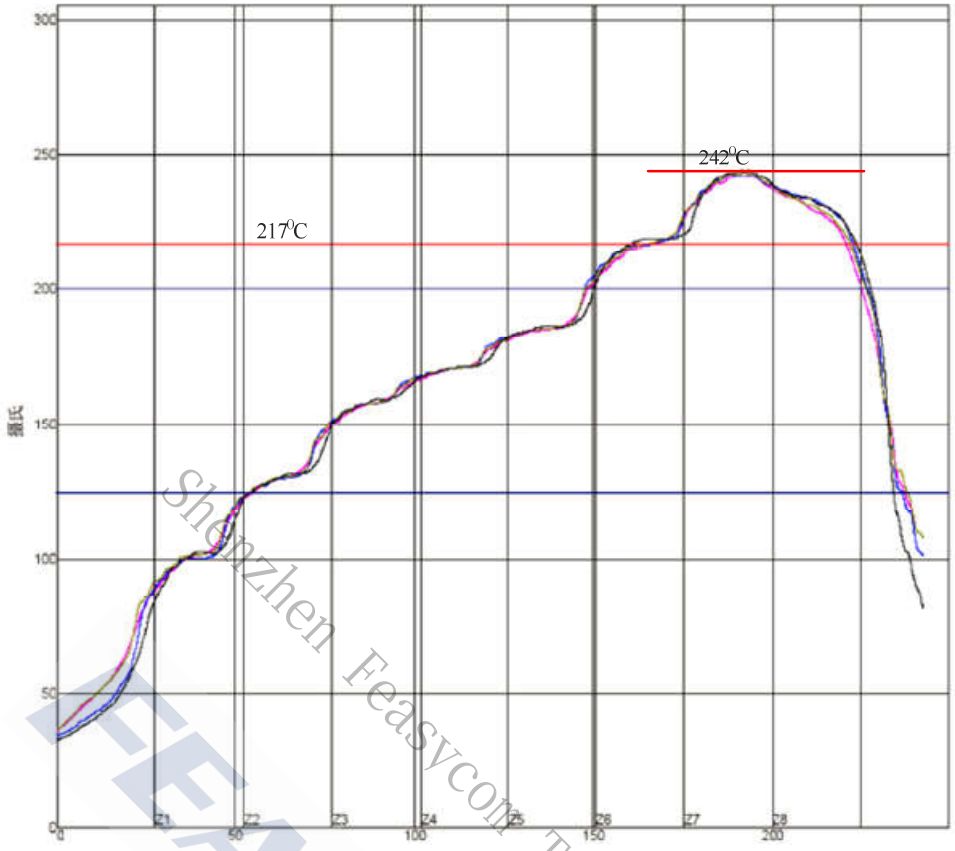

Figure 12 Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow. FSC-BT803 will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －40℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －40℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation Test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop Test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging Information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT803 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding via separated max 3 mm apart at the edge of grounding areas

to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND via all around the PCB edges.

The mother board should have no bare conductors or via in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or via) are allowed in this area, because of mismatching the on-board antenna.

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground via around it. Locate them tightly and symmetrically around the signal via. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

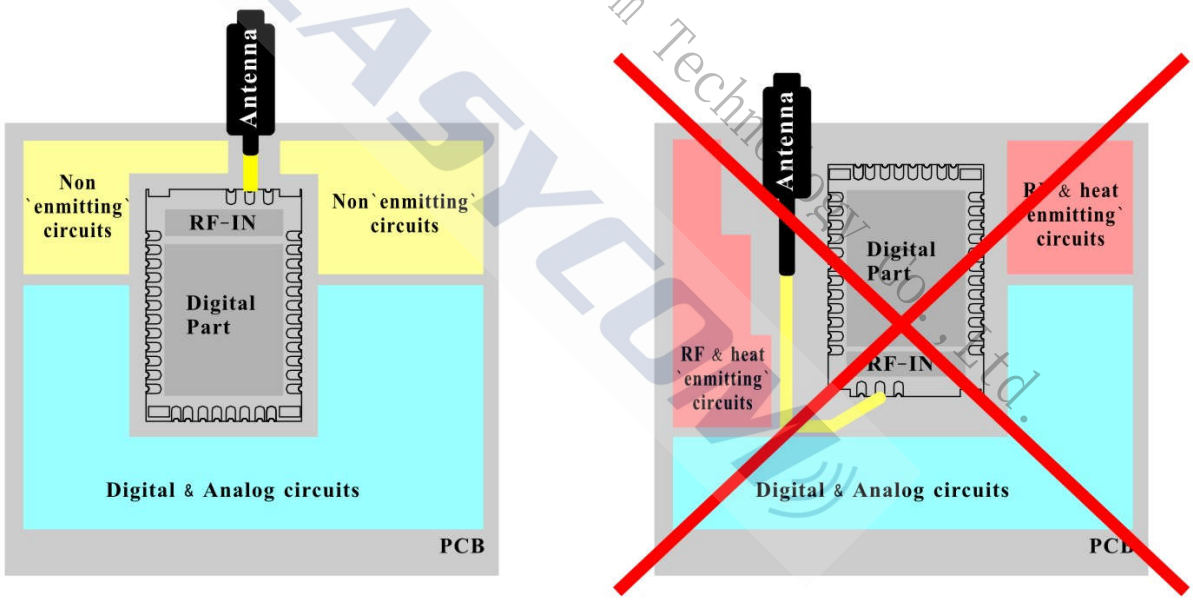

Figure 13: Placement the Module on a System Board

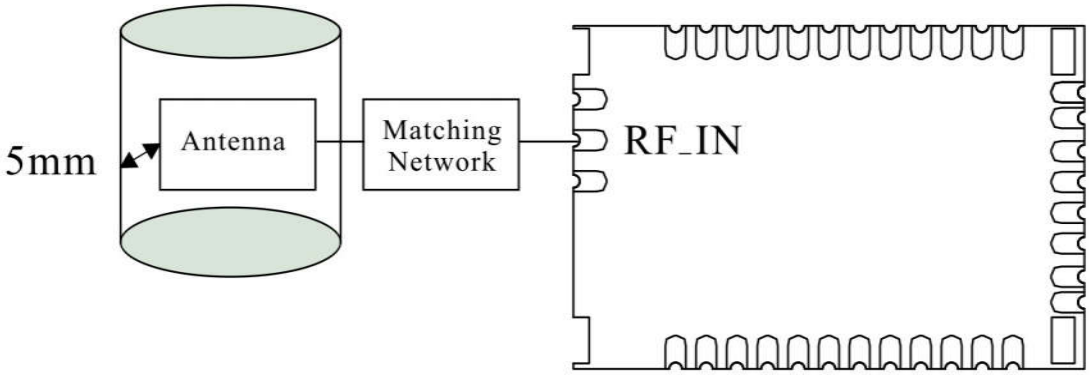

Figure 14: Leave 5mm Clearance Space from the Antenna

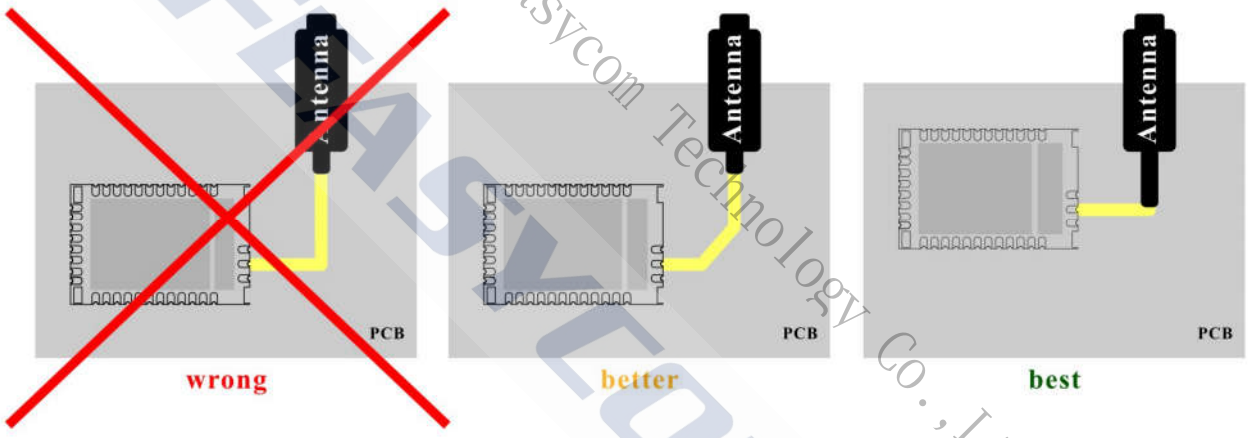

Figure 15: Recommended Trace Connects Antenna and the Module

9. Application Schematic